On-Chip Delay Measurement for Degradation Detection And Its Evaluation under Accelerated Life Test

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***Abstract*— Periodical delay measurement in field is useful for not only detection of delay-related faults but also prediction of faults due to aging. Logic BIST with variable test clock generation enables on-chip delay measurement in field. This paper addresses a delay measurement scheme based on logic BIST and gives experiment results to observe aging phenomenon of test chips under accelerated life test. The measurement scheme consists of scan-based logic BIST, a variable test clock generator, and digital temperature and voltage sensors. The sensors are used to compensate measured delay values for temperature and voltage variations in field. Evaluation using SPICE simulation shows that the scheme can measure a circuit delay with resolution of 92 ps. The delay measurement scheme is also implemented on fabricated test chips with 180 nm CMOS technology and accelerated test is performed using ATE and burn-in equipment. Experimental results show that a circuit delay increased 552 ps when accelerated the chip for 3000 hours. It is confirmed that the on-chip delay measurement scheme has enough accuracy for detection of aging-induced delay increase.**

Keywords*— *Field test, Logic BIST, Delay measurement, Degradation detection, Aging sensor, Accelerated life test

I. INTRODUCTION

VLSIs are widely used in various systems that require high reliability, such as automobiles, aircraft or social infrastructure. As issues that threatens the reliability of VLSIs, there are physical faults such as wiring disconnection or breakdown of gate oxide film due to aging, and transient faults that occur accidentally due to radiation effects [1]-[3]. Because some VLSI systems are used for a long term in various environments, avoidance of aging-induced faults is getting more and more important especially for safety critical applications [4][5]. There are several well-known aging phenomena such as EM (Electro-Migration), HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), and BTI (Bias Temperature Instability). HCI, NBTI (Negative BTI) and PBTI (Positive BTI) are known as aging phenomena that cause increase of a circuit delay [6]-[8]. Since the aging speed depends on a temperature and on-state ratio or switching activity of transistors during operation, it is hard to predict its degradation amount accurately in design phase [9]. Although usually 3-5 percent delay degradation is taken into a design margin, it may be too much or too less for each chip because of process variation. Such an inappropriate margin results in performance loss or an aging-induced fault, respectively [9][10]. When the circuit delay increases in field and exceeds an allowable range, the circuit malfunctions. Thus, in order to guarantee high reliability of VLSIs, it is desired to measure a circuit delay in field and to predict a delay-related fault due to aging before it occurs.

Various test methods for delay degradation detection have been proposed [11]-[17]. In [11] an aging sensor that consists of two flip-flops and an OR gate is inserted into the end of the longest combinational path (critical path) in a user circuit. The sensor outputs a warning signal when a delay in the critical path exceeds an amount determined in advance. A built-in BTI monitor [12] implemented on IBM's z196 Enterprise Systems consists of a reference oscillator and an oscillator that degradation in field. An on-chip aging monitor [13] consists of a ring-oscillator and a delay-line. The monitor has the advantages of small area and short measurement time. However, the sensors [11]-[13] detect only aging of specific paths and cannot detect aging of a whole circuit.

As for delay measurement, several methods have been proposed [18]-[22]. In the method in [18], BIST is inserted for critical paths identified by a static timing analyzer. The method in [20] measures a path delay with a time-to-digital-converter and a ring-oscillator (RO). In [21] and [22], on-chip delay measurement for degradation detection is realized as an in-field test architecture. The method, which is based on BIST with a variable test clock generator, measures a delay of paths sensitized by pseudo-random test patterns. The variable test clock generator can change an interval of a test clock, and allows us to check the delay of the sensitized paths by repeating a test with different test timing. The method can observe the delay increases due to aging in field.

For delay measurement in field, it is known that temperature and voltage give an impact on measured delay of the chip. In field, a temperature of the place where a chip is used is usually uncontrollable and a voltage supplied from the power source may also not be stable. In general, high temperature increases the circuit delay, while high voltage decreases it. Thus, in order to compare circuit delays measured at different time, the influence on the delay by the temperature and voltage variations should be eliminated. A concept of on-chip delay measurement scheme with correction for temperature and voltage variations was proposed in [21][22]. The scheme includes a delay measurement circuit combining logic BIST with a variable test clock generator [21][24] and a temperature and voltage sensor

[20]. However, it has not been verified whether the delay measurement method can detect real degradation, and its accuracy and/or feasibility have not been discussed.

In this work, to investigate the effectiveness of the on-chip delay measurement scheme, the delay measurement circuit is designed and fabricated, and then experiments using the test chips were done for observing aging phenomenon in an accelerated life test. In evaluation using SPICE simulation for the designed circuit, it is confirmed that a resolution of the delay measurement is 92 ps. Accelerated life test for the chips is performed using automated test equipment (ATE) and burn-in equipment. As a high stress condition, a heating temperature is set to 125 °C and over 2.80 V is applied though a standard core voltage is 1.80 V. Through the experiments, it is confirmed that the increased delay due to aging can be observed by the delay measurement circuit and that the on-chip delay measurement scheme has enough accuracy for detection of aging-induced delay increase. For example, a circuit delay increased 552 ps when accelerated the chip for 3000 hours. Note that, this paper focuses only on degradation evaluation, and it does not deal with a correction of effects of temperature and voltage for the measured delay.

This paper is organized as follows. Section II introduces the delay measurement and the RO-based sensor. Section III describes a chip with 180 nm CMOS technology. Section IV shows the effectiveness of the delay measurement by evaluation with accelerated life test. Section V concludes this paper.

II. On-Chip Delay Measurement for In-field Test

A. Logic BIST-based Delay Measurement [21]

As a dependable VLSI test architecture, an on-chip delay measurement method for degradation detection has been proposed [21], whose concept is illustrated in Figure 1. The method aims at avoiding delay-related failures caused by aging phenomenon like NBTI, HCI and TDDB. These are known that degrade performance of the chip gradually as time elapses. The method allows us to observe the aging-induced delay increases, that is the decrease in the delay margin, by repeatedly measuring the delay in field.

The delay measurement method [21] employs a variable test clock generator and a temperature and voltage sensor in addition to scan-based logic BIST. Pseudo-random test patterns generated by a TPG of logic BIST are applied for a circuit under test with an LoC (Launch-off-Capture) manner an interval between launch and capture signals to the same speed as a system clock interval initially. As the variable test clock generator can control the interval between the launch and capture signals, the same test patterns are applied again in shorter test clock intervals than the initial one as long as the test does not fail. Thus, a path delay in the circuit can be measured by repeatedly applying the test with different test clock. Since a measured delay in-field is influenced of temperature and voltage during measurement, the measured delay cannot be compared directly with another delay measured under different temperature and voltage. In order to compare the measured delay independently of the environmental factors, a correction for the measured delay is necessary for temperature or voltage when measured. A temperature and voltage sensor [23] is embedded to eliminate the influence of the environmental factors from the measured delay according to a correction mechanism developed [24].

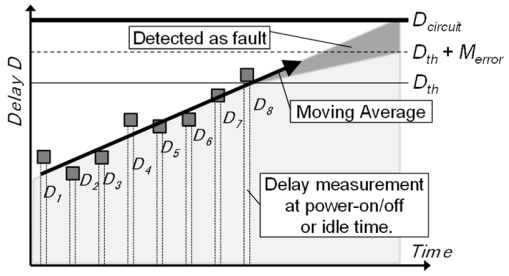


Fig. 1. Delay measurement for degradation detection in-field [21]

B. RO-Based Temperature and Voltage Sensor[23]

A digital temperature and voltage sensor (TVS) using ring oscillators (ROs) was proposed for in-field test [23]. The sensor consists of three types of ROs, which have different frequency characteristics each other with respect to temperature and voltage. The sensor calculates both a temperature and a voltage from the measured RO frequencies simultaneously. When the sensor is used for a long time in field, its measurement accuracy may decrease due to aging of the sensor itself. The aging such as electro-migration or HCI can be avoided by stopping oscillation of an RO. However, even if the RO stops oscillation, the transistors deteriorates due to NBTI. An NBTI-tolerant RO structure, which is shown in Figure 2, has been proposed in [23]. The aging model for NBTI indicates that degradation progress while a PMOS transistor is in on-state [9][10]. When the structure as shown in Figure 2 is adopted, the PMOS transistors related to oscillation will be off-state during non-oscillation mode, it can be NBTI-tolerant. The RO needs to oscillate only while the sensor measures a temperature and voltage, and it can stop oscillation while not measuring. The measurement time of the sensor is about 10 μs per one measurement, which is 100 times faster than analog sensor's. Therefore, real-time performance equivalent to that of the analog sensors can be secured even for measurement every 1 msec.

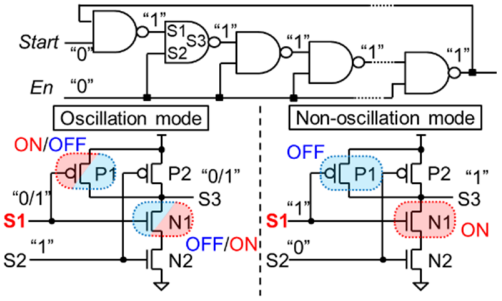


Fig. 2. NBTI-tolerant RO with two-input NAND gates [23]

C. Degradation Detection using Delay Measurement [24]

A correction method [24] of temperature variation using delay measurement and the temperature sensor [23]. How much the delay increased due to aging can be calculated from a difference between the initial delay and the corrected measured delay. By logging the measured delay in internal or external memory, the amount of degradation is count from the stored delay data. Therefore, degradation detection can be done by comparing the delay at different times.

III. Evaluation with Test Chips

A. Test Chip Architecture

In order to look into the feasibility of the degradation detection method described in the previous section, test chips are designed. A test chip is designed with 180 nm CMOS technology, the core voltage is 1.80 V, the I/O voltage is 3.3 V, the chip size is 5 mm square. Figure 3 and Table I show a test chip architecture and main functions mounted on the chip, respectively. An embedded PLL and SRAMs are foundry provided IPs. The circuit under test is OpenCores minSoC [25], in which a standard scan design is taken using commercial EDA tools. Then, typical logic BIST is constructed by connecting an LFSR as a TPG, and a MISR as a response analyzer (RA) to the CUT. Two CUTs are implemented to consist the chip with multiple clock domains. The variable test clock generator is designed based on a method using delay difference between multiple delay elements as explained in the next subsection. The TVS consists of three pair of RO and counter, and four TVSs are mounted on the chip. The test controller that manages an entire test circuit, an internal memory used to store test conditions or results, and an I/O controller are also mounted. The number of manufactured test chips is eight.

Figure 4(a) shows a test chip layout, where the black area in the center is circuits such as CUTs. Figure 4(b) shows a test chip image. The variable test clock generator or the temperature and voltage sensor are designed as hard macros by manual layout, in order to reduce process variations including delay variations due to place and routing. On the other hand, others circuits such as controllers or CUTs are designed by automatic place and routing.

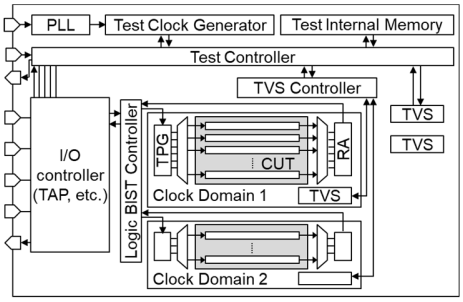
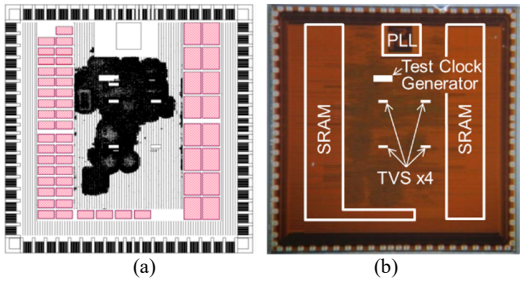


Fig. 3. Test chip architecture.

TABLE I. Main Functions Mounted on the Test Chip

Module	#Gates	Description	Note
Test Controller	16.0k	Controller of entire test architecture	-
Test Internal Memory	-	Storage of test condition and result	SRAM
Test Clock Generator	0.6k	Generation of variable test clock	-
TVS Controller	0.7k	Controller of RO oscillation	-
TVS	5.5k	Temperature and voltage sensor	3 ROs x 4 Units
Logic BIST (TPG, RA, ets.)	3.0k	Logic BIST architecture	Without CUT
CUT	57.5k	Circuit under test	CUT is minSoC



(a) (b)

Fig. 4. Test chip in 180 nm CMOS technology (5 mm square).

B. Variable Test Clock Generator

A variable test clock generator as shown in Figure 5 is designed which changes an interval between two clock signals using delay difference among multiple delay elements. An input clock passes through two variable delay paths, two output clocks *TCLK_L* and *TCLK_C* are used as capture and launch signals in logic BIST, respectively. The variable delay path consists of buffer chains, and the number of the buffers through which the clock passes can be controlled by a parameter *DLYC*. The number of buffers corresponding to *DLYC* are 2^0, 2^1, 2^2, ... , 2^{i-1} for i = bit of *DLYC*. Since the implemented *DLYC* has 8-bits, the delay amounts are $1(2^0)$, $2(2^1)$, $4(2^2)$, ..., $128(2^7)$. For example, when *DLYC* are set to all 0s, the clock passes through four selectors in the variable delay path. When it is set to 10110000, the output clock delayed by 7 buffers in addition to the selectors. *TCLK_L* used as the launch signal can pass through a delay path including some buffers. On the other hand, capture clock *TCLK_C* always passes through a delay path such that *DLYC* is set to all 0s. Thus *DLYC* can delay *TCLK_L*, the interval between launch and capture signals can be shortened as shown in Figure 6. Since the test timing becomes smaller by shortening the interval, it suggests that the test clock become faster.

SPICE simulation was used for evaluation of the variable test clock generator. Table II shows results of a variable delay path. The amount of delay per one bit in *DLYC* that is equivalent to one stage of buffer can be calculated from the amount of delay variation when the parameters of the variable delay path are changed. It was confirmed that a resolution of the variable delay path was 92 ps.

Evaluation for manufactured test chips was also done in which a resolution of the variable delay path was calculated from a boundary of pass/fail results in logic BIST. This evaluation is similar to description with shmoo-plot that is a function of an ATE commonly used to measure the system performance of chips. Table III shows results for a variable delay path. First, the pass/fail boundary was checked. It was confirmed and found that the boundary was between the clock periods 98.8 ns and 108.1 ns. Then, the boundary was checked again when the *DLYC* was changed from 68 to 78. Since the boundary occurred when the number of buffers increased 10 stages, the delay of the variable delay path can be calculated. It was confirmed that a resolution, which is equivalent to one stage of buffer on the variable delay path, was 116.25 ps.

Note that, when the variable clock generator deteriorates, it has a great effect on an accuracy of the delay measurement. As a countermeasure for degradation, it is important to stop the operation by clock gating or to shut off the power by power gating when the variable clock generator is not used.

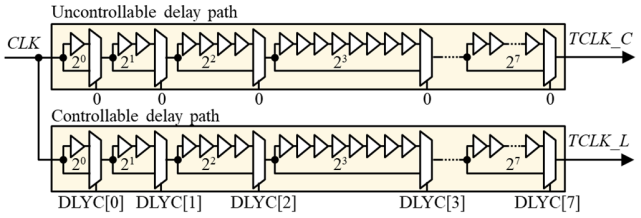


Fig. 5. Variable delay paths in the variable test clock generator

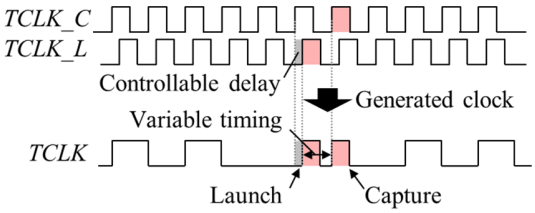


Fig. 6. Waveform of the variable test clock generation

TABLE II. EVALUATION ON VARIABLE DELAY PATH BY SIMULATION

DLYC	#Buffer	Rise [ns]	Fall [ns]	Ave. [ns]	Increase [ns]	Step [ns]
00000000	0	2.131	2.023	2.077	-	-
10000000	1	2.216	2.123	2.169	0.092	0.092
01000000	2	2.302	2.223	2.262	0.093	0.093
00100000	4	2.462	2.426	2.444	0.182	0.091
00010000	8	2.830	2.824	2.815	0.371	0.093
00001000	16	3.479	3.635	3.557	0.742	0.093
00000100	32	4.830	5.226	5.028	1.471	0.092
00000010	64	7.552	8.509	8.031	3.003	0.094
00000001	128	12.893	14.943	13.918	5.887	0.092

TABLE III. EVALUATION ON VARIABLE DELAY PATH OF A CHIP

DLYC	Pass/Fail boundary period[ns]	PLL output clock period[ns]	Clock period difference[ns]	Resolution per one buffer [ps]
68	98.8	12.35	1.16	116.25
78	108.1	13.51	-	-

C. NBTI-tolerant Ring Oscillator

The implemented temperature and voltage sensor consists of the following three ROs; RO1 has 33 stages of 2-input NAND with fan-out of 1, RO2 has 7 stages of 4-input ORNAND with fan-out of 6, and RO3 has 15 stages of 2-input EXOR with fan-out of 1. The first stage of each RO uses a 3-input NAND as a common structure for oscillation control. The number of RO stages are designed so that RO frequencies become about 150 to 300 MHz. Since the ROs are designed to have an NBTI-tolerant structure [23], NBTI does not progresses in the non-oscillation mode. A setting oscillation time of the ROs is about 81.92 μs (4096 clocks) when a system clock is 50 MHz. The oscillation time is much shorter than a time of non-oscillation mode, the aging due to switching activity during oscillation mode will negligible.

IV. EVALUATION WITH ACCELERATED LIFE TEST

The effectiveness of degradation detection for the delay measurement circuit is evaluated by observing aging phenomenon in accelerated life test, which are called accelerated degradation test or long-term reliability test.

A. Experimental Setup

In accelerated life test, ATE used for semiconductor manufacturing test and burn-in equipment are used. Aging is accelerated by exposing the chips under high stress condition. This test uses test conditions related to a high-temperature operating life (HTOL), which is one of the accelerated life test for semiconductors. Time of accelerated life test is not 1000 hours which is that of generally performed by chip foundry, but 3000 hours to observe degradation more apparent. The detailed stress conditions are as follows:

Condition 1) From 0 to 2000 hours, temperature and voltage are 125 °C and 2.80 V, respectively. Note that standard core voltage is 1.80 V. Delay measurement in the test mode is performed under 45 °C and 1.80 V that are the typical test conditions.

Condition 2) From 2000 to 3000 hours, temperature and voltage are 125 °C and 3.00 V, respectively. The aging is accelerated further by increasing the voltage to 3.0 V. The purpose of the condition is to confirm whether the difference in the aging degree due to the difference in stress conditions can be observed.

Figure 7 shows a relation between chip operation and stress conditions during the accelerated life test. In order to reproduce an aging phenomenon in user operation, random patterns are applied to the CUT to activate it. Since the CUT always operates, aging of the CUT is accelerated. The additional circuits for testing such as a delay measurement circuit or a temperature and voltage sensor do not run during the user mode. ROs of the sensor does not oscillate, but high stress is applied for the ROs. Run time of the user mode is over 100 hours. On the other hand, in test mode, normal test operations including scan testing of logic BIST, delay measurement, temperature and voltage measurement using the sensor, are performed under typical test conditions. The ROs of the sensor oscillate during 81.92 μs. Run time of the test mode is less than 100 ms.

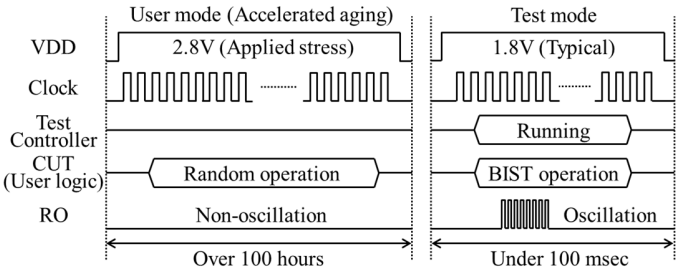


Fig. 7. Chip operation during accelerated life testing

B. Degradation Evaluation of NBTI-tolerant Ring Oscillator

Degradation of NBTI-tolerant ROs mounted as a temperature and voltage sensor is evaluated. Figure 8 and Table IV show relations between the measured RO count value and the elapsed time in the accelerated life test. When the RO deteriorates, the RO count value decreases because a delay of transistor increases. In RO1 of Chip2, the initial RO count was 30,793, and the RO count at 2000 hours was 30,818. In this experiment, decrease in the RO count due to degradation was not observed. Since the RO count fluctuated during measurement are about ± 0.1% compared to the initial RO count, it is considered that it fluctuated due to measurement variations. In RO2 and RO3 as well as RO1, decrease in the RO count value due to degradation could not be observed. In other chips, the absolute value is different due to process variation, but decrease in the RO count value due to degradation could not be observed as well as chip 2. Therefore, the evaluation result suggests that the NBTI-tolerant ROs can suppress the degradation progress and have NBTI-tolerant structure for the sensor.

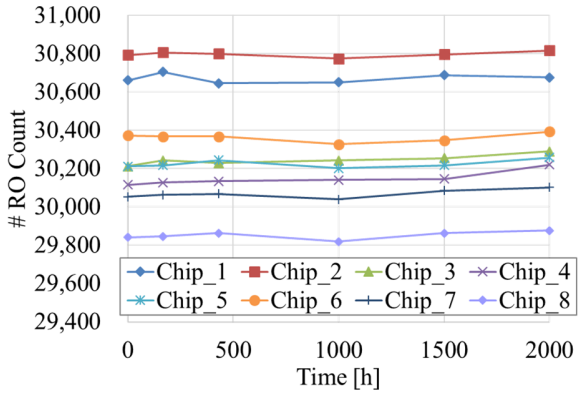


Fig. 8. Evaluation of the NBTI-torelant ROs (eight chips, RO1)

TABLE IV. EVALUATION OF THE ROS (EIGHT CHIPS, RO1)

	Measured RO count values (RO1)					
Time [h]	0	168	430	1000	1500	2000
Chip 1	30,662	30,706	30,647	30,651	30,688	30,676
Chip 2	30,793	30,808	30,800	30,775	30,797	30,818
Chip 3	30,213	30,243	30,229	30,243	30,255	30,291
Chip 4	30,116	30,128	30,134	30,141	30,147	30,221
Chip 5	30,213	30,217	30,244	30,202	30,218	30,259
Chip 6	30,374	30,369	30,368	30,328	30,348	30,394
Chip 7	30,053	30,064	30,069	30,040	30,085	30,103
Chip 8	29,841	29,846	29,864	29,819	29,863	29,877

C. Degradation Evaluation using Automated Test Equipment

In this section, results for delay measurement are shown using shmoo-plot which is a function of ATE. The input clock is generated by the ATE, and a pass/fail boundary of logic BIST is investigated by changing the clock period. The delay can be computed from the period and the boundary. Then, to observe an aging of the delay with accelerated life test.

Figure 9 and Table V show relations between a measured delay using the shmoo-plot and the elapsed time in the accelerated life test. The resolution of shmoo-plot is 12.5 ps, and it depends on the ATE. Although the number of test chips is eight, data of the first 430 hours for four chips are missing due to an ATE trouble. For Chip 2, the initial delay is 9.125 ns, the delay at 430 hours is 9.388 ns (263 ps increase), and a delay at 2750 hours is 9.600 ns (475 ps increase). From the measured results, it was confirmed that the CUT deteriorated by the accelerated life test, and the increased delay can be observed by the ATE. After 2000 hours, the degradation was further accelerated under higher stress conditions, and speed-up of degradation could be observed. Although the absolute values in each chips are different due to process variation, increase in the measured delay due to degradation were observed as well as Chip 2. While the delay of the CUT has increased due to aging, the RO evaluation results in Section IV-B show that degradation of the RO has not progressed even after 2000 hours. Thus, the evaluation results of the delay measurement suggest that the effectiveness of the NBTI-tolerant RO can be confirmed again.

D. Degradation Evaluation using Delay Measurement Circuit

In order to evaluate the effectiveness of degradation detection by an on-chip delay measurement circuit, a delay measurement is performed using the variable test clock generator and the logic BIST. Then, the aging of the CUT delay accelerated by the accelerated life test is measured using the delay measurement circuit. A resolution of the variable test clock generator uses 92 ps that is an evaluated value with SPICE simulation as shown in Section III-B. A pass/fail boundary of the logic BIST is investigated by sequentially changing a parameter of the variable test clock generator. A delay of the CUT can be computed from the parameter of when the boundary is found.

Figure 10 and Table VI show the relation between the measured delay using the on-chip delay measurement and the elapsed time in the accelerated life test. In the chip 2, An initial delay is 9.188 ns, a delay at 430 hours is 9.464 ns (276 ps delay increase), and a delay at 2750 hours is 9.740 ns (552 ps delay increase). Also, it was confirmed that a difference in the degree of degradation due to more high stress conditions of after 2000 hours from the measured values. As well as Chip 2, increase in the measured delay due to degradation were observed using the on-chip delay measurement circuit. Therefore, the evaluated results show the delay increase due to the degradation of the user logic circuit can be measured by the delay measurement circuit.

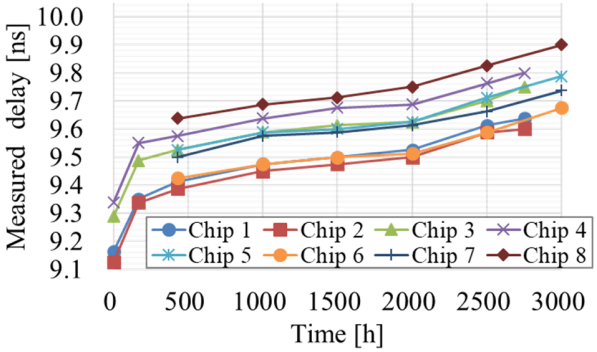


Fig. 9. Degradation observation by shmoo-plot (using ATE)

TABLE V. DEGRADATION OBSERVATION BY SHMOO-PLOT

	Measured delay [ns]								
Time [h]	0	168	430	1000	1500	2000	2500	2750	3000
Chip 1	9.163	9.350	9.413	9.475	9.500	9.525	9.613	9.638	-
Chip 2	9.125	9.338	9.388	9.450	9.475	9.500	9.588	9.600	-
Chip 3	9.288	9.488	9.525	9.588	9.613	9.625	9.700	9.750	-
Chip 4	9.338	9.550	9.575	9.638	9.675	9.688	9.763	9.800	-
Chip 5	-	-	9.525	9.588	9.600	9.625	9.713	-	9.788
Chip 6	-	-	9.425	9.475	9.500	9.513	9.588	-	9.675
Chip 7	-	-	9.500	9.575	9.588	9.613	9.663	-	9.738
Chip 8	-	-	9.638	9.688	9.713	9.750	9.825	-	9.900

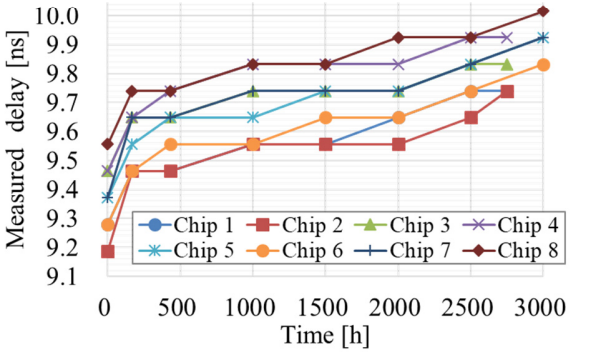


Fig. 10. Degradation observation by on-chip delay measurement.

TABLE VI. DEGRADATION OBSERVATION BY ON-CHIP MEASUREMENT

	Measured delay [ns]								
Time [h]	0	168	430	1000	1500	2000	2500	2750	3000
Chip 1	9.280	9.464	9.464	9.556	9.556	9.648	9.740	9.740	-
Chip 2	9.188	9.464	9.464	9.556	9.556	9.556	9.648	9.740	-
Chip 3	9.464	9.648	9.648	9.740	9.740	9.740	9.832	9.832	-
Chip 4	9.464	9.648	9.740	9.832	9.832	9.832	9.924	9.924	-
Chip 5	9.372	9.556	9.648	9.648	9.740	9.740	9.832	-	9.924
Chip 6	9.280	9.464	9.556	9.556	9.648	9.648	9.740	-	9.832
Chip 7	9.372	9.648	9.648	9.740	9.740	9.740	9.832	-	9.924
Chip 8	9.556	9.740	9.740	9.832	9.832	9.924	9.924	-	10.016

E. Effectiveness Evaluation of Degradation Detection

Table VII shows a comparison of the measured delay by the on-chip delay measurement circuit and that of by the shmoo-plot. Since the same CUT in the same chip is measured, the theoretical circuit delay is the same value. However, there is a difference of 140 ps in the measured delay in the results shown in Table VII. The difference is an amount of about 1 or 2 steps of the resolution 92 ps in the variable test clock generator. Resolution differs between the on-chip delay measurement and the shmoo-plot measurement. Although there are differences in resolutions and the effect of measurement errors, it was confirmed that the measured delay values of the on-chip delay measurement and the shmoo-plot measurement were similar values. Therefore, the evaluation result suggests that the same effect as the measurement by the ATE can be realized on-chip measurement. Then, it could be confirmed that the effectiveness of degradation detection by on-chip delay measurement circuit.

TABLE VII. COMPARISON OF SHMOO-PLOT AND ON-CHIP MEASUREMENT

#Chip 2	Measured delay [ns]							
Time [h]	0	168	430	1000	1500	2000	2500	2750
Shmoo plot	9.125	9.338	9.388	9.450	9.475	9.500	9.588	9.600
On-chip Measure.	9.188	9.464	9.464	9.556	9.556	9.556	9.648	9.740
Difference	0.063	0.127	0.077	0.106	0.081	0.056	0.048	0.140

V. CONCLUSIONS

In this paper, in order to evaluate the feasibility of on-chip delay degradation detection method that realizes highly reliable VLSIs in field, an on-chip delay measurement circuit was prototyped and evaluated using an accelerated life test. The test chip is designed with 180 nm CMOS technology, the effectiveness of degradation detection using the delay measurement circuit was evaluated by the accelerated degradation for the chips using a burn-in equipment. It was confirmed that the increased delay can be measured by the on-chip delay measurement. The experiment also suggests that the same effect as the measurement by the ATE can be realized on-chip measurement. Therefore, it could be confirmed that the effectiveness of degradation detection by on-chip delay measurement circuit. As future works, in order to observe more aging phenomenon including PBTI, evaluation using a finer chip such as 40 nm CMOS technology are planned.

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