On-Chip Delay Measurement for In-Field Test of FPGAs

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Abstract— **Avoidance of delay-related failures due to aging phenomena is an important issue of current VLSI systems. Delay measurement in field is effective for detection of aging-induced delay increase. This paper proposes a delay measurement method using BIST (Built-In Self-Test) in an FPGA. The proposed method consists of variable test timing generation using an embedded PLL, BIST-based delay measurement, and correction of the measured delay with reflecting temperature variance in field. In on-chip delay measurement of the proposed method, the fastest operating speed is checked by repeating delay test with several test timings. Because circuit delay is influenced by temperature during measurement, the measured delay is then corrected according to the temperature during testing. Based on test log including the corrected delay, delay degradation and aging detection can be grasped. In evaluation experiments of the propose method implemented on an Intel Cyclone IV FPGA device (60nm technology), variable test timing generation realized 96 ps timing step resolution (that is below 1% of the system clock), correction process for measured delay could reduce influence of temperature variation. Furthermore, its feasibility of the proposed method for aging detection is discussed in this paper.**

Keywords— **FPGA, Field test, Periodic Test, Delay measurement, Deterioration detection, Temperature sensor.**

I. INTRODUCTION

In order to guarantee high reliability of state-of-the-art VLSI systems, testing and monitoring in-field have been introduced [4], [5]. Especially, measurement of a circuit delay is effective, and periodical delay measurement in-field is useful for not only fault detection but also fault prediction. However, the VLSI systems are used in various environments, and a temperature of the place where the VLSI systems are used is often uncontrollable. It is known that the temperature gives an impact on circuit delay of the chip. In general, high temperature increases the circuit delay, and low temperature decreases it. Therefore, in order to compare the measured delay at different times, the influence on the delay by the temperature variation should be eliminated. Furthermore, the VLSI systems are used long-term in various environments, and avoidance of aging-induced failures is an important issue of the VLSI systems. There are several well-known aging phenomena such as EM (Electro-Migration), HCI (Hot Carrier Injection), and BTI (Bias Temperature Instability). Negative BTI (NBTI) and Positive BTI (PBTI) are known as aging phenomena that cause increase of a circuit delay [6], [7]. If the increased delay exceeds an allowable delay limit, a system failure might occur.

FPGAs are widely used in various embedded systems due to their re-configurability, flexibility, and reduced time-to-market. Demand for versatile FPGAs is increasing as compared to ASICs. Even for safety-critical systems and mission-critical systems such as automotive or social infrastructural systems, the FPGAs are being employed [1]-[3], while aging phenomena happen in the FPGAs.

FPGA testing methods are classified into two categories: application-independent testing and application-dependent testing [8], [9]. Application-independent testing, which is done by an FPGA manufacturer or a vender, aims at checking for the entire FPGA. On the other hand, application-dependent testing, which is done by an FPGA user, aims at checking implemented functions for used logic blocks and interconnect resources of the user circuit [9]-[19]. The methods in [10]-[12] realize 100% fault coverage for any single fault model such as open, stuck-at or bridging faults of the user circuit by re-configuring it with a test-specific circuit. Test methods using BIST (Built-In Self-Test) without re-configuration have been proposed in [9] and [13]. The BIST method in [13] inserts test points for the user circuit into unused resources. Many researches on delay testing and delay measurement for FPGAs have been done [14]-[17]. The method in [16] measures a path delay using a time-to-digital-converter (TDC) and a ring-oscillator (RO). The comparison-based delay test methods in [13] and [19] perform delay testing by the difference of the arrival time of several paths having the same structure and delay values.

Various test methods for degradation detection have been proposed. The aging sensor in [20] consists of two flip-flops (FFs) and an OR gate. The sensor is put onto the termination of the longest combinational path (critical path) in the user circuit. Then, if the delay of the critical path that increased by aging exceeds a predetermined value, it outputs a warning signal. The sensor takes very simple architecture with small area and low power. However, since the sensor detects only an aging of the critical path, it cannot detect an aging of a whole circuit, nor measure the progress of aging.

This paper proposes a delay measurement method for FPGAs. The delay measurement scheme, which is applicable to in-field test, consists of variable test timing generation using an embedded PLL (Phase-Locked Loops), BIST-based delay test, and correction of the measured delay with reflecting temperature variance in field. The method is supposed to be applied at a power-on, power-off, or idle time of the system in-field. In general, it is difficult to know the delay of assigned logic blocks and interconnect wires of FPGAs and to predict the delay increase due to aging. In on-chip delay measurement, the fastest operating speed is checked by repeating delay test with several test timings in field. Because circuit delay is influenced by temperature during measurement, the measured delay is then corrected according to the temperature during testing. Based on test log including the corrected delay, delay degradation and aging detection can be grasped.

Experiments in implementing the proposed method on an Intel Cyclone IV FPGA device (60nm technology [21]) show that a timing step resolution of variable test timing generation is 96.15 *ps* (that is below 1% of the system clock). It is confirmed that the proposed delay measurement method makes it possible to measure the path delay of the circuit. A path delay in the experiments was 8942.35 ps in 70 ℃, and the relation between the measurement delay and temperature was 7.34 [ps/℃]. Correction process for measured delay could reduce influence of temperature variation. Furthermore, its feasibility of the proposed method for aging detection is discussed in this paper.

This paper is organized as follows. Section 2 describes the concept of delay measurement in-field. Section 3 describes on variable test timing used in the proposed method. Section 4 describes delay measurement with correction processing for temperature influence. Section 5 shows experimental results using an Intel Cyclone IV device. Section 6 concludes this paper.

II. PRELIMINARIES

A. *Delay Measurement for Degradation Detection* [17]

Figure 1 explains the concept of on-chip delay measurement for degradation detection that has been proposed as a dependable VLSI test architecture [17,18]. The method proposed in [17] mainly targets delay-related failures caused by aging such as NBTI, HCI and TDDB. NBTI, which degrades PMOS transistor performance, is a well-known aging phenomenon. The performance of the chip gradually degrades as time elapses. Some aging models for NBTI indicate that degradation progresses while the PMOS is active [6], [22]. Since the aging speed depends on temperature and on-state ratio of each transistor during operation, it is hard to predict its degradation amount [23]. Usually 3-5 percent delay degradation is taken into a design margin [23, 24]. It may be too much or too less, and brings performance loss or an aging-induced fault, respectively. The aging speed and delay margin can be known accurately by repeatedly measuring with time and care in-field.

The method in [17], which was developed for ASICs/SoCs, utilizes standard DFT such as scan and logic BIST as much as possible. Additional design to the standard DFT consists of a variable test timing generator and a temperature sensor. In BIST-based delay testing, a path delay in the circuit can be measured by repeatedly measuring the delay with different test timing. The variable test timing generator generates clock signals with an arbitrary interval by shifting a system (normal) clock signal. Since a measured delay in-field is influenced of temperature during measurement, a measured delay cannot be compared directly with another delay measured under different temperature. In order to compare measured delay values independently of temperature, a correction for the measured delays must be made. Thus, temperature sensors [25], [26] are embedded and used to exclude the influence of temperature from the measured delay. The ROs have an aging-tolerant structure in order to use a long-term in-field [27].

The test method in [17] has the following three major operational modes; production test mode, user functional mode, in-field periodic test mode. The production test mode is a mode where a manufacturing test commonly performed using ATE (Automated Test Equipment). The user functional mode is a mode where a user function is executed. The in-field periodic test mode is a mode where a delay measurement or logic BIST are executed in-field like power-on self-test. By switching among these modes, the system can keep high field reliability. By using the delay measurement method, the delay increase that brings reduction of the delay margin can be observed. Therefore, the method is useful to avoid a sudden system failure due to aging.

Note that, the design structure for delay measurement in [17] is equipped not only logic BIST but also memory BIST, test access ports (TAP), some embedded memories to keep test information, a controller for field test. This paper focuses on structure for the delay measurement.

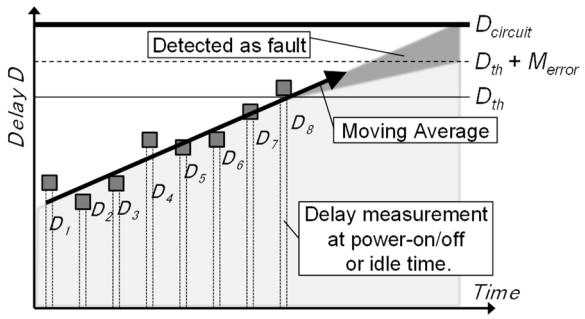

Figure 1. Delay measurement for degradation detection in-field [17]

B. *Test Clock Generation for Logic BIST*

In BIST-based delay testing, since test clock generation and control have very important role, many techniques for clock generation have been proposed. In [28], a high-speed on-chip test clock generation technique is given for delay test of SOC devices with multiple clock domains. It has discussed on a method of synchronizing a test timing in multiple clock domains, or a method to realize synchronization between a high-speed clock generated by an on-chip PLL and low-speed clock supplied from an external tester. In [29], a clock generation method for improving test quality from the ATPG tool perspective is proposed. In [30], an on-chip clock generation scheme for faster-than-at-speed delay testing is proposed in which a timing difference between launch and capture signals is reduced using the delay difference of multiple delay elements. A method in [31], which is a technique to generate a capture signal on-chip with a programmable delay, realizes a faster-than-at-speed delay testing. However, these methods are developed for ASIC/SoC devices and could not be applied for FPGAs directly.

C. *Issues for FPGA Implementation*

In ASIC/SoC design, it is possible to estimate circuit delay including wire delay or gate delay with simulation. On the other hand, in FPGA design, it is difficult to estimate the delay of assigned logic blocks and interconnect wires. For example, although an ASIC can be designed so that the delay amount of multiple delay elements used for a clock generator is the same, it cannot be designed in FPGAs. Thus, the variable test timing generators for ASICs/SoCs are not able to be implemented in FPGAs nor to achieve required accuracy/resolution, and it is required to develop a variable test timing generator for a delay measurement in FPGAs.

III. On-Chip Delay Measurement on FPGAs

A. BIST-based At-speed Delay Testing

Figure 2 shows a design structure for delay measurement using logic BIST on an FPGA. Figure 3 shows a test timing of LoC (Launch-off-Capture) scheme at-speed delay testing for scan circuits. When the SE (Scan-Enable) is set to 0, launch and capture clocks are applied. At-speed delay testing can be performed by adjusting the interval between the launch and capture cycles to the same speed as the system clock interval. The test timing generator in Figure 2 generates test clock with a variable interval between the launch and capture cycles. The TS (Temperature Sensor) is a temperature sensor [26] that is used for measurement of chip temperature at the time of testing. The test timing generator in Figure 2 generates test clock with a variable interval between the launch and capture cycles. The TS (Temperature Sensor) is a temperature sensor [26] that is used for measurement of chip temperature at the time of testing.

Note that fault coverage by logic BIST depends on test patterns which are generated by a pseudo-random pattern generator such as an LFSR (Linear Feedback Shift Register). The test patterns or seeds of the LFSR are set so as to achieve high fault coverage.

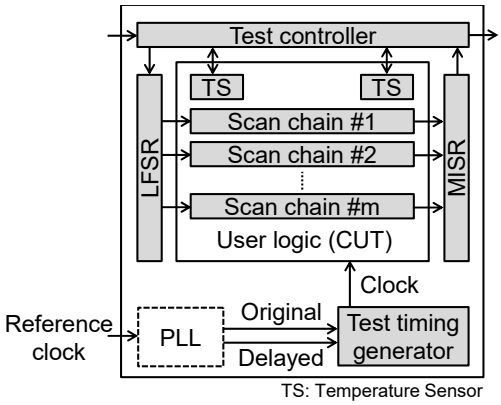

Figure 2. Design structure of delay measurement with LBIST

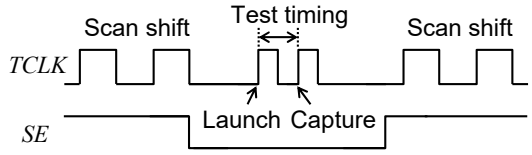

Figure 3. Test timing of Launch-off-Capture

B. Variable Test Timing Generation

In BIST-based delay testing of the proposed method, a path delay of a CUT can be measured by changing the test timing. This section addresses a technique of variable test timing generation to measure a path delay in an FPGA.

An embedded PLL in an FPGA has a dynamic phase shift function that can delay a phase of an output clock of the PLL in real time without re-configuration. Resolutions of the dynamic phase shift function, which is a controllable minimum step value, depends on a voltage-controlled oscillator (VCO) of the PLL [21]. The proposed method utilizes two output clocks of the PLL using the phase shift function to generate variable test timings as shown in Figure 4. One output clock is the original clock for the capture cycle. The other clock is a controllable clock for the launch cycle.

Figure 5 shows waveforms of the variable test timings. $SCLK$ is a scan clock; CLK is the original clock of the PLL. $DCLK_i(i = 0,1,2,\dots,N)$ is a controllable clock using the phase shift function, where N is the number of times that performed phase shift, and PS is a controllable minimum step value of phase shift. $TCLK_i$ is a generated test clock, and it is the same period as the $SCLK$ during the shift mode. On the other hand, during the capture mode, one cycle of $DCLK_i$ is used as the launch cycle, and one cycle of CLK is used as the capture cycle. Then, t_i is a generated test timing which corresponds to a period between the launch by $DCLK_i$ and the capture cycle by CLK.

At first, initialization of the PLL and phase shift of the PLL are performed. $DCLK_0$ is adjusted toward the original clock CLK to be the same as the test timing of the system clock. The first test timing t_0 of $TCLK_0$ is the same speed as the normal function. When phase shift is performed one time, the t_1 of $DCLK_1$ is delayed an amount of PS. Then, a relation between the number of phase shift and the generated test timing is shown as follow:

$$t_N = initial\ clock - (PS * N) \qquad (1)$$

By repeating phase shift, the test timing becomes smaller, that is, the test clock become faster. Thus, the proposed test timing generator can realize the variable test timing for the BIST-based delay testing.

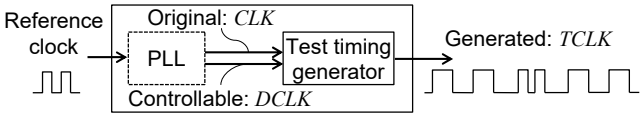

Figure 4. Design structure of test timing generation.

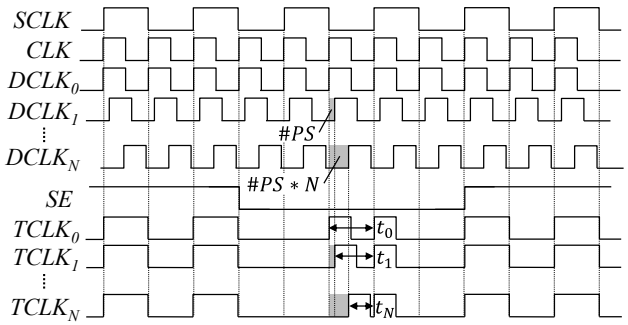

Figure 5. Waveform of variable test timing

C. Delay Measurement using Variable Test Timing

Figure 6 shows the delay measurement flow using the variable test timing. $t_i(i = 0,1,2,\dots,N)$ is a variable test timing that is utilized at the BIST-based delay testing; a Pass/Fail decision is made for each t_i. N is the upper limit of phase shift that is decided in advance. $t_{fastest}$ is the fastest test timing such that the test result is "Pass". The details of the delay measurement flow are shown in the following.

***1) Initialization of clock generator**:* Initialization of a PLL and phase shift of the PLL are performed. t_0 and $t_{fastest}$ are set to the same value that is used as an initial clock. When the

initial clock is the system clock, the first test is performed as at-speed testing.

2) BIST operation*:* At first, general initialization of BIST is performed before delay testing. Secondly a generated test pattern by an LFSR is inserted into scan-chains. Then, scan shift operation or capture operation are performed. The generated test clock, which has the controllable test timing t_i, is used at the capture operation. A Pass/Fail decision is made for each pair of generated test patterns and t_i. As long as the result is Pass, it suggests that the user circuit would have enough delay margins or timing margins corresponding to t_i. On the other hand, if the result is Fail, it suggests that the user circuit would not have the margins corresponding to t_i. If the circuit passed a test with t_i, the circuit is tested with faster timing t_{i+1}.

3) Timing update operation*:* Before updating the timing of t_i, it keeps a timing of t_i to $t_{fastest}$ as the fastest test timing for which a test result is pass. Then, phase shift is performed, and the test timing is updated t_i to t_{i+1}. The updated t_i is decreased the amount of *PS*, which is the controllable minimum step value of the phase shift function, as the following equation:

$$t_i = t_0 - (PS * i) \qquad (2)$$

Thus, the variable test timing t_i is getting smaller and smaller by repeating the timing update operation.

4) Repetition of 2) and 3)*:* After the test timing updated, BIST operation is performed again with the test timing. By repeating BIST and timing update operations until the fail result is detected, the fastest test timing can be found.

Thus, the proposed delay measurement method using variable test timing can measure the fastest operating speed for test patterns used in BIST. As a result, the performance of user circuits such as delay margins, timing margins, or delay variation due to process variation, can be measured.

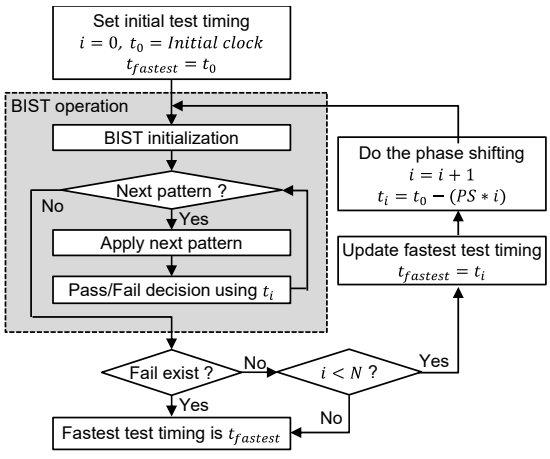

Figure 6. Flow of the delay measurement with variable test timing

IV. Delay Measurement with Correction of Temperature Influence

Since a measured delay in field is influenced of temperature variation, the measured delay cannot be compared with one measured at a different time. Thus, influence of delay variation due to temperature change must be eliminated for temperature-independent delay measurement. Furthermore, the measured delay is not only varied by temperature variation but also increased by an aging. This section discusses a relation among the measured delay, the temperature and the aging, and proposes a correction technique of temperature influence for the measured delay.

A. Temperature Influence for the Measured Delay

Figure 7(a) shows a relation between the measured delay and the temperature. D_0 is a delay as a reference that is measured at the initial measurement under a well-controlled condition in regard to temperature. Temperature T_0 at the initial measurement is assumed that it is known value. ΔD_T is a varied delay due to the temperature variation ΔT. D_T is a delay that is sum of D_0 and ΔD_T. The relation between the measured delay and the temperature is shown as follows:

$$\Delta D_{\mathrm{T}} = \alpha * \Delta T \qquad (3)$$

$$D_{\mathrm{T}} = D_0 + \Delta D_{\mathrm{T}} = D_0 + \alpha * \Delta T \qquad (4)$$

where α is a temperature coefficient for delay. Because the relation of the delay variation for the temperature variation is derived by circuit simulation and preliminary measurement, the influence of temperature for the measured delay can be corrected using a temperature measurement. If degradation did not occur, corrected delay $D_{Corrected}$ must be the same value as an initial delay D_0, because measured delay $D_{Measured}$ in field consists of initial delay D_0 and delay variation ΔD_T due to temperature. The relation among the measured delay, the corrected delay, and the temperature are shown in the following equations.

$$D_{Measured} = D_0 \pm \Delta D_T = D_0 \pm (\alpha * \Delta T) \qquad (5)$$

$$D_{Corrected} = D_0 = D_{Measured} \mp \Delta D_T = D_{Measured} \mp (\alpha * \Delta T) \qquad (6)$$

Therefore, the value of delay variation due to the temperature variation can be calculated from the measured temperature and the temperature coefficient for delay. Then, the corrected delay, which is independent of temperature, can be calculated from the measured delay in field and the calculated delay variation.

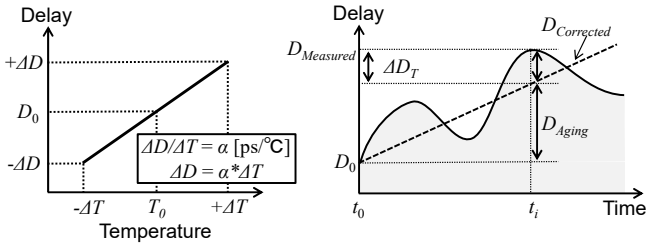

Figure 7. Relation between the measured delay, the temperature, and the delay increasing due to aging in field.

B. Detection of Delay Increase by Aging

When a system is used a long term in field, the delay increases by aging phenomena. Figure 7(b) is shown a

relation between the measured delay, temperature, and aging. In the case of considering aging, the measured delay $D_{Measured}$ in field includes the increased delay due to D_{Aging} not only the initial delay D_0 and the delay variation ΔD_T. The relation is shown as follows:

$$D_{Measured} = (D_0 + D_{Aging}) \pm \Delta D_T \quad (7)$$

$$\begin{aligned} D_{Corrected} &= (D_0 + D_{Aging}) \\ &= D_{Measured} \mp \Delta D_T \\ &= D_{Measured} \mp (\alpha * \Delta T) \end{aligned} \quad (8)$$

$$D_{Aging} = D_{Corrected} - D_0 \quad (9)$$

The influence of temperature for the measured delay can be corrected as well as Equation (5) using the temperature as shown in Equation (8) where the corrected delay $D_{Corrected}$ includes the initial delay D_0 and the increased delay D_{Aging}. Therefore, the value of the delay due to aging can be calculated from the initial delay and the corrected delay, detection of aging can be realized by comparing the delay at different times.

C. Delay Measurement with a Temperature Sensor

The proposed delay measurement method employs a temperature sensor for correction of the measured delay so as to remove the influence of delay variation by temperature. Figure 8 shows a structure for delay correction processing. The delay measurement circuit with the variable test timing generator measures a path delay and outputs initial delay D_0 and measured delay $D_{Measured}$. The temperature sensor measures an on-chip temperature and outputs initial temperature T_0 and measured temperature ΔT. The delay correction processing module calculates the delay $D_{Corrected}$, which is independent of temperature, using Equation (8) and (9). Parameters forcalculation such as α are stored in a nonvolatile memory.

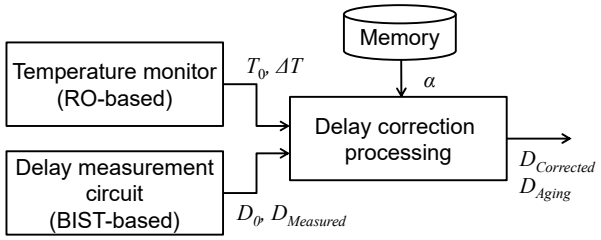

Figure 8. Delay correction processing

V. Evaluation with a FPGA

A. Experimental Setup

An Intel Cyclone IV FPGA device (60 nm technology) is used for experiments to make ure the effectiveness of the proposed method. A controllable minimum step resolution of the dynamic phase shift, which depends on VCO frequency of the embedded PLL in the FPGA [21], is about 96.15 *ps*. . The initial clock of the test timing generator is 100 MHz. As a CUT B13 (ITC'99 benchmark circuit) is selected, and buffer chains to give an extra delay were inserted to the original B13, because the original delay of B13 was too small to evaluate the proposed method.

B. Evaluation of Variable Test Timing

In order to evaluate actual accuracy of the phase shift step resolution of the test timing generator, the generated test timing is observed with an oscilloscope. A phase difference between the original clock and the controlled clock is observed using a Lissajous waveform obtained with the oscilloscope as shown in Figure 9. Figure 10 shows the phase difference that is generated by the test timing generator. Ideal values are calculated from the step resolution determined by the embedded PLL. When the phase shift count reached to 20 times, an average of error, which is the difference between the measured and the ideal values, was -20.10 *ps*, and INL (Integral Non-Linearity) was within ±10 %.

Therefore, it was confirmed that the proposed test timing generator can generate the variable test timing and can continue to generate smaller and smaller test timings. Note that, in order to validate the variable test timing, an on-chip test clock validation technique using a TDC (Time-to-Digital Converter) in FPGAs have been proposed [32].

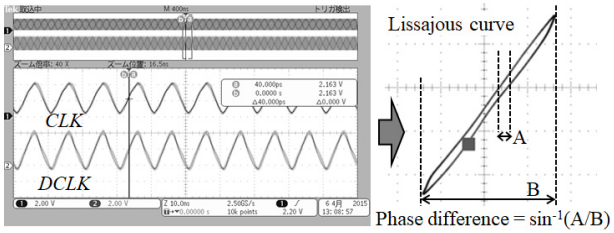

Figure 9. Observation of the phase difference between an original and a controllable clocks using Lissajous waveform.

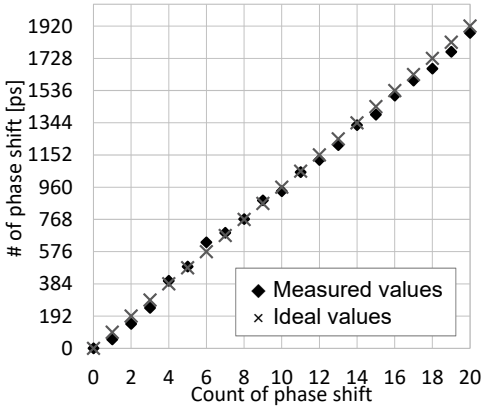

Figure 10. Observation of variable test timing with an oscilloscope

C. Evaluation of Delay Measurement with Variable Test Timing

The initial clock is 100 MHz and the initial test timing is 10,000 *ps*. Table 1 shows Pass/Fail results of 32 test patterns at each step. The number of executions of phase shift is 49. Since all values of scan-out of the 1st pattern are initial values, Pass/Fail decision is not made for the 1st pattern. In this experiment, when the amount of phase shift is 769.20 *ps*, "Fail" was detected. It means that the timing margin of the circuit is less than 769.20 *ps* and the fastest test timing which a test result becomes "Pass" is the previous timing 673.05 *ps*. This result suggests that the lower bound of the delay is 9326.95 *ps*. Table 1 also shows that the timing of "Fail" is different depending on test patterns. (e.g. 865.35 *ps* for the 4th test pattern of phase shift, and 1634.55 *ps* for the 2nd test pattern of

phase shift.) This is because each test pattern determines paths to be tested. And once test result becomes “Fail” for a test pattern, results for the subsequent test patterns keep “Fail” because Pass/Fail is judged by the signature of the MISR.

TABLE I. PASS/FAIL RESULTS WITH VARIABLE TEST TIMING

Step		0	1	~	7	8	9	~	16	17	~	49
Phase Shift [ps]		0	96.15	~	673.05	769.20	865.35	~	1538.40	1634.55	~	4711.35
Delay[ps]		10000.00	9903.85	~	9326.95	9230.80	9134.65	~	8461.60	8365.45	~	5288.65
Pass/Fail (MISR output)		*P*	*P*	~	*P*	*F*	*F*	~	*F*	*F*	~	*F*
# of Test Pattern	1	-	-	~	-	-	-	~	-	-	~	-
	2	*P*	*P*	~	*P*	*P*	*P*	~	*P*	*F*	~	*F*
	3	*P*	*P*	~	*P*	*P*	*P*	~	*P*	*F*	~	*F*
	4	*P*	*P*	~	*P*	*P*	*F*	~	*F*	*F*	~	*F*
	~	~	~	~	~	~	~	~	~	~	~	~
	10	*P*	*P*	~	*P*	*P*	*F*	~	*F*	*F*	~	*F*
	11	*P*	*P*	~	*P*	*F*	*F*	~	*F*	*F*	~	*F*
	~	~	~	~	~	~	~	~	~	~	~	~
	32	*P*	*P*	~	*P*	*F*	*F*	~	*F*	*F*	~	*F*

P: Pass, *F*: Fail

D. Evaluation of Delay Variation due to Temperature

In order to evaluate the delay measurement method under various temperatures, experiments are performed using a thermostatic bath, Espec SU-241. The temperature range is from 40 ℃ to 100 ℃ that is within the range of the recommended operating condition of the FPGA device, an error of the PLL due to temperature variation is negligible [21].

In order to know a chip temperature during delay measurement, a RO-based temperature sensor [26] is also implemented on the chip. Figure 11 shows a relation between a setting temperature using the thermostatic bath and a measured temperature by the sensor. The measured temperature was calculated from frequencies of the ROs in the sensor. For a temperature range from 40℃ to 100℃, the measured temperature error, which is a standard deviation of the residuals, was 1.40℃.

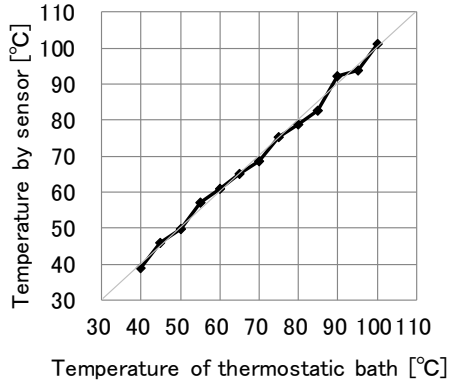

Figure 11. Evaluation of a temperature sensor

Figure 12 shows a relation between the measured delay and the measured temperature. The temperature values in the Figure are not the setting values of the thermostatic bath but the sensor values. The delay increases with the increase of temperature. For the temperature range from 40℃ to 100℃, the delay range was from 8750.05 *ps* to 9230.80 *ps*. The measured delay was shown as a stepwise function because the phase shift step resolution is 96.15 *ps*. A dotted line in Figure 12 shows the real delay estimated from a relation between the measured delay and the phase shift step resolution. The relation between the real delay and the temperature can be expected to be linear.

Table 2 shows the delay variation due to temperature variations. Assuming that the initial temperature T_0 is 70 ℃, the initial delay D_0 is 8942.35 *ps*. A temperature sensitivity α, which is a temperature coefficient for the delay, is 7.34 [ps/℃], and the delay varies 0.08% per 1℃.

Thus when the relation of the delay variation for the temperature variation is known by circuit simulation or a preliminary measurement, the influence of temperature for the measured delay can be corrected from the parameters by combining with temperature measurement.

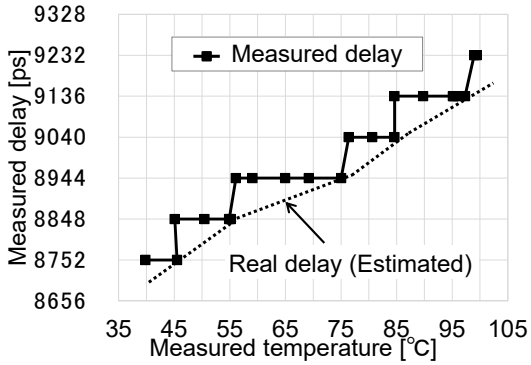

Figure 12. Observation of variable test timing with an oscilloscope

TABLE II. DELAY VARIATION DUE TO TEMPERATURE VARIATION

Delay: D_0 [*ps*] (T_0: 70℃)	Temperature sensitivity: α [*ps*/℃]	
8942.35	7.34	0.08%

E. Evaluation of Temperature Correction Processing

Figure 13 shows experiment results of the correction of temperature influence. The solid line indicates pre-correction values that are the same values as in Figure 12. The dotted line indicates post-correction values that are corrected for the pre-correction values using the proposed correction processing of temperature influence. An initial temperature at the time of the initial measurement is 70 ℃, and the initial measured delay is 8942.35 *ps*; that is, (T_0, D_0) is (70 ℃, 8942.35 *ps*). The initial values become reference points for the correction.

Table 3 also shows the results of delay measurement with temperature correction. The maximum and minimum values with respect to D_0 in pre-correction are 288.45 *ps* and -192.30 *ps*, respectively. The range of the delay variation due to the temperature variation is 480.75 *ps*. On the other hand, the maximum and minimum values with respect to the D_0 in post-correction are 105.65 *ps* and -34.43 *ps*, respectively. The range of the delay variation due to the temperature variation is 480 *ps*. Thus, it is confirmed that the delay variation due to the temperature variation is reduced from 480.75 *ps* to 140.08 *ps* by the proposed correction processing.

Thus, the proposed delay measurement method can measure the delay which is corrected temperature influence for the delay in field. A system using the proposed delay measurement method can compare the measured delay at different times. Then, the system can guarantee a performance of user circuits by repeatedly applying the delay measurement for the circuits without re-configuration in field.

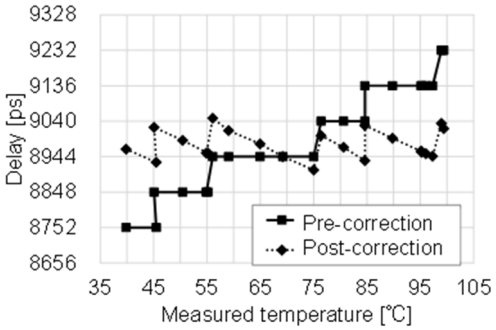

Figure 13. Delay measurement under variable temperature

TABLE III. DELAY MEASUREMENT WITH TEMPEARTURE CORRECTION

	Initial	Pre-correction			Post-correction		
	(T_0, D_0)	Max.	Min.	Range	Max.	Min.	Range
Delay [*ps*]	8942.35	9230.80 (+288.45)	8750.05 (-192.30)	480.75	9048.00 (+105.65)	8907.92 (-34.43)	140.08

F. Further discussion

VLSI systems are sometimes used long-term in various environments. The progress of aging is different depending on operating environment and the operating status. By performing the delay measurement repeatedly, a delay increase due to aging would be able to be caught. However, when a user circuit has not aged yet, the circuit delay which is measured by the proposed method, keeps near the initial measured value (T_0, D_0). In order to evaluate feasibility of the proposed method, it is important to measure values that affected by actual aging. For example, an experiment under a high temperature by the thermostatic bath would be effective as an accelerated test. Then, it will be expected to detect a delay increase due to aging. In order to realize degradation detection using the proposed method, evaluation using the accelerated test still remains as a future work.

VI. CONCLUSIONS

This paper proposed a novel delay measurement method consisting of variable test timing generation and BIST-based delay measurement. The proposed delay measurement makes it possible to measure the fastest operating speed for given test patterns. The performance of the user circuit denoted by delay margins, timing margins or delay variation due to a process variation can be measured without re-configuration in-field. Furthermore, this paper also proposed a correction technique of temperature influence for the measured delay using a temperature sensor. The correction technique has an important role for highly accurate delay measurement independent of temperature variation. Experimental results using the Intel Cyclone IV FPGA device (60nm technology) showed that the timing step resolution of delay measurement is about 96.15 *ps* (below 1% of system clock). It implies that a change of the performance during VLSI operation can be observed by iterative delay measurement. Then, the experiments confirmed that an influence of temperature for the measured delay can be corrected by combining with temperature measurement. The experiments suggest that it would be able to observe the delay increase due to aging caused by long-term use in various environments. Therefore, the proposed method will be useful to guarantee high reliability for FPGAs in-field.

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