Path Delay Measurement with Correction for Temperature And Voltage Variations

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Abstract— **Path delay measurement in field is useful for not only detection of delay-related faults but also prediction of aging-induced delay faults. In order to utilize the delay measurement results for fault detection and fault prediction, the measured delay must be corrected because the circuit delay is varied in field due to environment such as temperature or voltage variations. This paper proposes a method of BIST-based path delay measurement in which the influence of environmental variations is eliminated. An on-chip sensor measures temperature and voltage during delay measurement. Using information from the temperature and voltage sensor and pre-computed temperature and voltage sensitivities of the circuit delay, the measured delay value is corrected to a delay value that would be obtained under a fixed temperature and voltage. Evaluation for a test chip with 65nm CMOS technology implementing the proposed method shows that errors of measured delays brought by environmental variations could be reduced from 2419 to 211 ps in the range of 30 to 80 °C and 1.05 to 1.35 V. This paper also discusses application and feasibility for degradation detection of the proposed method.**

Keywords— Field test; Logic BIST; Delay measurement; Degradation detection; Temperature and voltage variation;

I. INTRODUCTION

VLSIs have been widely used in systems that require high reliability, such as automotive, medical or social infrastructure. In order to guarantee the high reliability of state-of-the-art VLSI systems, design and test methods for dependability have been introduced [1][2]. Path delay measurement in field is often done as power-on self-test for the purpose of not only detection of delay-related faults but also prediction of aging-induced faults [3][4]. As the VLSI systems are used in various environments, a temperature or a voltage of the place where the VLSI systems are operating is often uncontrollable. In general, high temperature increases the circuit delay, and low temperature decreases. As for the voltage, high voltage decreases the circuit delay, while low voltage increases it [5][6]. The varied delay due to the temperature and voltage variation causes not only malfunction of the system but also causes erroneous results in delay testing. Therefore, it is necessary to correct the measured delay value according to the temperature and voltage at the time of measurement. In particular, since automotive systems are used over a wide temperature range, a correction for temperature variation is very important. For example, an ambient temperature near an automotive engine will be above 125 °C [7]. To guarantee the high reliability of the automotive VLSI systems in accordance with the functional safety ISO 26262 [8], it is necessary to achieve an environment-independent delay measurement.

As for delay measurement, various methods have been proposed [9]-[15]. In the method in [9], logic BIST is employed for testing critical paths identified by a static timing analyzer. The method of [10] measures a path delay by inserting a delay-sensor circuit to the internal nodes of logic blocks using an approach for on-die delay sensing and test point insertion. The method of [11] measures a path delay with a time-to-digital-converter and a ring-oscillator (RO). The method of [12] measures a path delay with a time-to-digital-converter utilizing a Vernier delay line. The method of [13] measures a path delay with signature registers for small-delay defect detection. The method of [14] measures a delay to be used for dynamic voltage and frequency scaling (DVFS) using multiple delay paths with different characteristics. The method of [15] based on BIST with variable test clock generation measures a delay of paths sensitized by pseudo-random test patterns with sequentially changing intervals of a test clock. Most of these methods measure path delay that includes the effects of temperature and voltage variations.

Furthermore, some VLSI systems are used long-term in various environments, and avoidance of delay-related faults due to aging is getting more and more important for the state-of-the-art VLSI systems. There are several well-known aging phenomena such as EM (Electro-Migration), HCI (Hot Carrier Injection), TDDB (Time Dependent Dielectric Breakdown), and BTI (Bias Temperature Instability) [16]-[18]. The HCI, NBTI (Negative BTI) and PBTI (Positive BTI) are aging phenomena that cause increase of a circuit delay. If the delay increases due to aging and exceeds the allowable delay limit, a circuit malfunction or a system failure may occur. Since the aging speed depends on operating environments and usage conditions, it is difficult to predict the amount of degradation. Therefore, in order to guarantee the high reliability of VLSIs, it is desired to measure a circuit delay in field with considering environments variations and to predict the occurrence of delay-related fault due to aging.

Various test methods for delay degradation detection also have been proposed [19]-[22]. In [19] an aging sensor that consists of two flip-flops and an OR gate is inserted into the terminal of the longest combinational path (critical path) in the user circuit. Then, it outputs a warning signal when the delay of the critical path exceeds the pre-determined value. A monitor [20] consists of a pair of programmable delay circuits and it measures the degradation from the delay difference. A built-in BTI monitor [21] consists of a reference oscillator and an oscillator that degradation in field. An on-chip aging monitor [22] that consists of a ring-oscillator-type monitor and a delay-line type monitor. It has the advantages of small area and short measurement time. However, since the sensors detects only aging of specific paths, they cannot detect aging of a whole circuit. Also, because the delay varies with the temperature and voltage during testing, It is not possible to know the progress of the degradation by comparing the measured delay value to the previously measured delay values. To compare the delay values measured at different times, it is required to correct the valued such that the influence of temperature and voltage variations is eliminated from the measured delay values.

A path delay measurement scheme with correction for temperature variation was proposed in [15]. Its feasibility was evaluated for FPGAs using a delay measurement circuit

combining logic BIST with a variable test clock generator [15][23] and a temperature sensor [24]. The effectiveness of degradation detection was evaluated using accelerated life test [25] The previous works have aimed at correction only for temperature variation and it have not considered for voltage variations. For ultra-fine CMOS technology, a threshold voltage of transistors is lower and the impact of voltage variation on circuit delay is larger. Therefore, it is necessary to take on account of not only the effects of temperature variation but also of voltage variation.

This paper proposes a method to correct delay values measured in field for temperature and voltage variations. The proposed method analyzes temperature and voltage characteristics of circuit delay in advance, and expresses the characteristics as a polynomial approximation for correction processing. Since the characteristics are not linear, accurate correction can be realized by using polynomial approximation. In evaluation using a fabricated test chip with 65nm CMOS technology, some results show that the proposed method can reduce the influence of in-field environmental variations from 2419 to 211ps in the ranges of 30 to 80°C and 1.05 to 1.35V. This paper also discusses application and feasibility for degradation detection based on the delay values that are independent of the environmental variation.

This paper is organized as follows. Section II introduces the delay measurement in field. Section III proposes a correction method of delay values to reduce an influence of temperature and voltage variations to delay measurement. Section IV shows a test chip evaluation with 65 nm CMOS technology. Section V concludes the paper.

II. On-Chip Delay Measurement for In-field Test

A. Logic BIST-based Delay Measurement [15]

As a dependable VLSI test architecture, an on-chip delay measurement method for delay degradation detection has been proposed [15]. The method aims to avoid failures caused by aging phenomenon such as NBTI, HCI and TDDB that degrades chip performance gradually as time elapses. The method allows us to observe an increase in a delay due to aging, that is a decrease in a delay margin, by repeatedly measuring the delay in field.

The delay measurement method [15] embeds a variable test clock generator and a temperature and voltage sensor in addition to scan-based logic BIST. In logic BIST, pseudo-random test patterns are generated for a circuit under test with an LoC (Launch-off-Capture) manner. An clock interval between launch and capture signals is initially set to the same as a system clock interval. As the variable test clock generator controls the interval between the launch and capture signals, the same test patterns are applied again in shorter test clock intervals than the initial one as long as the test does not fail. When a pass/fail result is a pass, it suggests that the user circuit would have enough delay margins corresponding the clock interval. When the pass/fail result is a fail, lower bound of the delay margin, or a path delay can be computed. Thus, the path delay can be measured by repeatedly applying the test with a different test clock interval.

Since a measured delay in field is affected by environmental factors such as temperature and voltage during measurement, the measured delay cannot be compared directly with another delay measured under a different temperature and voltage. Furthermore, the delay is not only varied due to temperature or voltage variations but also increased due to aging. In order to compare the measured delay independently of the environmental factors and to detect the increased delay due to aging, it is required to correct temperature and voltage influences from the measured delay.

B. Temperature and Voltage Characteristic for Delay

A circuit delay is varied depending on a temperature and voltage. In CMOS technology in 65nm process or more, the circuit delay increases when a temperature increases, and the delay decreases when a voltage increases. However, the circuit delay may decrease when a temperature increases in an ultra-fine CMOS technology such as 20nm or less.

Logic BIST can test paths with the maximum delay among the paths sensitized by test patterns. Since the temperature and voltage characteristics of a circuit delay are different for each path, the path of maximum delay may change depending on the temperature and voltage at the time of testing. Figure 1 illustrates an image of a relation between a delay and a voltage. When a measurement target is a specific path for a fixed test pattern , the characteristic may be close to linear because it depends on the temperature and voltage sensitivity of one path as shown in Figure 1(a). On the other hand, as the logic BIST uses a large number of test patterns and the sensitized paths are changed for each test pattern. Since the path with the maximum delay changes depending on the temperature and voltage at the time of testing, the characteristics of the delay detected by the BIST-based delay measurements may not be linear as shown in Figure 1(b).

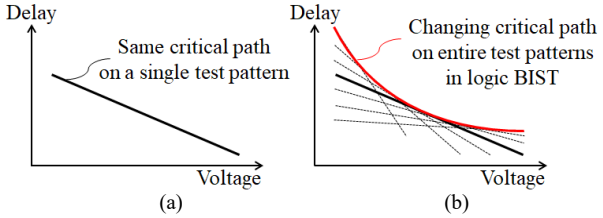


Figure 1. Relation between delay and voltage. (a) Same critical path on a specific path or a single test pattern. (b) Changing critical paths on entire test patterns in logic BIST.

C. Correction of Only Temperature Variation in FPGAs[23]

In order to correct temperature and voltage influences from the measured delay, a correction method [23] of temperature variation using a delay measurement and a temperature sensor [24] has been proposed, it was evaluated in a FPGA. The delay due to aging can be calculated from a difference between an initial measured delay and the corrected delay. The previous method is a correction method only for a temperature variation, and it does not consider the effect for voltage. Since, temperature and voltage variations in the field occur at the same time, a method that can correct both temperature and voltage effects is needed.

III. Correction of Temperature and Voltage Variations

A. Correction Method using Linear Approximation

In a field test, the environment at the time of the first measurement is an environment that is very well controlled with respect to temperature and voltage like a manufacturing test. Thus, it can be handled assuming that a temperature value and a voltage value at the first measurement are known.

Figure 2(a) and Figure 2(b) show relations between the delay and the temperature, the delay and the voltage in a field,

respectively. T_0 and V_0 are temperature and voltage values at the first measurement, and D_0 is a measured delay value under the environment in T_0 and V_0. ΔD_T is a delay value that changes when the temperature changes ΔT from T_0, ΔD_V is a delay value that changes when the temperature changes ΔV from V_0. α is a temperature coefficient, that is, a temperature sensitivity for the delay, which can be expressed as $\Delta D_T/\Delta T$ $[\,ps/℃\,]$ by using linear approximation. Thus, when the measured delay value in the field is $D_{Measured}$, the relation between the measured delay and the temperature can be expressed as the following equations (1) and (2).

$$\Delta D_T = \alpha \Delta T \tag{1}$$

$$D_{Measured} = D_0 + \alpha \Delta T \tag{2}$$

Also, β is a voltage coefficient, that is, a voltage sensitivity for the delay, which can be expressed as $\Delta D_V/\Delta V$ $[ps/mV]$ by using linear approximation. Thus, the relation between the measured delay and the voltage can be expressed as the following equations (3) and (4).

$$\Delta D_V = \beta \Delta V \tag{3}$$

$$D_{Measured} = D_0 + \beta \Delta V \tag{4}$$

When the relationship among the delay, the temperature, and the voltage is obtained using circuit simulation or actual chip measurement, the delay variation $(\Delta D_T + \Delta D_V)$ in the field can be calculated from temperature ΔT and voltage ΔV at the time of delay measurement. When the deterioration has not progressed, the delay value $D_{Corrected}$ that corrected by the temperature influence $\alpha\Delta T$ and the voltage influence $\beta\Delta V$ with respect to the measured delay value $D_{Measured}$ becomes the same value as the delay value D_0. The relation can be expressed as the following equations (5) and (6).

$$D_{Measured} = D_0 + \alpha \Delta T + \beta \Delta V \tag{5}$$

$$D_{Corrected} = D_0 = D_{Measured} - \alpha \Delta T - \beta \Delta V \tag{6}$$

The delay values in field can be measured using a delay measurement circuit [15][23], the temperature and voltage values at the time of the test in field can be measured using an on-chip temperature and voltage sensor [24]. Therefore, by knowing the temperature coefficient α and the voltage coefficient β with respect to the delay in advance, it becomes possible to correct the temperature and voltage influence from the measured delay using the temperature and voltage values at the time of the test.

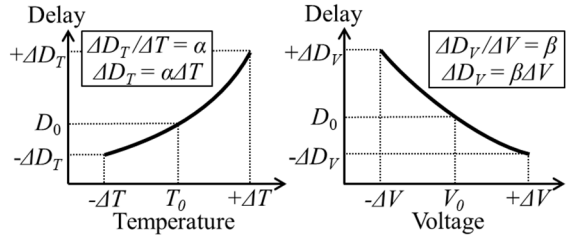


Figure 2. Relation between delay and temperature, and delay and voltage in commonly used CMOS technology such as 65nm.

B. Detection of Delay Increase due to Aging

Figure 3 shows a relation between the measured delay, the temperature, the voltage, and the delay increasing due to aging in field. Since the delay is not only varied by temperature or voltage variations but also increased by an aging, the measured delay value also includes the delay increase value D_{Aging} due to aging. The relation between equation (7) can be derived by correcting the temperature and voltage influence for the measured delay.

$$\begin{aligned} D_{Aging} &= D_{Corrected} - D_0 \\ &= D_{Measured} - D_0 - \alpha \Delta T - \beta \Delta V \end{aligned} \tag{7}$$

As a result, D_{Aging} can be expressed as the difference between the corrected delay value $D_{Corrected}$ and the initial delay value D_0 as follows:

$$D_{Corrected} = \left(D_0 + D_{Aging}\right) - \alpha \Delta T - \beta \Delta V \tag{8}$$

$$D_{Corrected} = D_{Measured} - \alpha \Delta T - \beta \Delta V \tag{9}$$

$$D_{Aging} = D_{Corrected} - D_0 \tag{10}$$

Therefore, the delay value due to aging can be calculated using the proposed method that correcting temperature and voltage influence from the measured value, degradation detection can be realized by comparing the delay at different times.

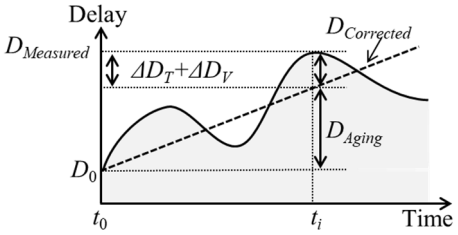


Figure 3. Relation between the measured delay, the temperature, the voltage, and the delay increasing due to aging in field.

C. Correction Method using Polynomial Approximation

The relations $\Delta D_T = \alpha \Delta T$ or $\Delta D_V = \beta \Delta V$ as shown in the previous section are derived using a linear approximation. However, the relations between delay, temperature, and voltage, that are, temperature and voltage characteristics of circuits are not linear in actual CMOS circuits. In particular, the characteristics in the BIST-based delay measurements are the curves shown in Figure 1(b). Thus, there is an issue that its approximation error is large when linear approximation is used. In order to realize a correction method suitable to the actual circuit characteristics, this section proposes a correction method of temperature and voltage influences using a quadratic polynomial.

The relation between the delay, the temperature, and the voltage shown in Figure 2 can be expressed as follow equations (11) and (12) using a quadratic polynomial.

$$\Delta D_T = \alpha_1 \Delta T + \alpha_2 \Delta T^2 \tag{11}$$

$$\Delta D_V = \beta_1 \Delta V + \beta_2 \Delta V^2 \tag{12}$$

Then, the relation between the measured delay, the corrected delay with respect to the temperature and voltage influences, and the delay increase due to aging are expressed as follows.

$$D_{Corrected} = D_{Measured} - \{\alpha_1 \Delta T + \alpha_2 \Delta T^2\} - \{\beta_1 \Delta V + \beta_2 \Delta V^2\} \tag{13}$$

$$\begin{aligned} D_{Aging} = D_{Measured} - D_0 - \{\alpha_1 \Delta T + \alpha_2 \Delta T^2\} \\ -\{\beta_1 \Delta V + \beta_2 \Delta V^2\} \end{aligned} \tag{14}$$

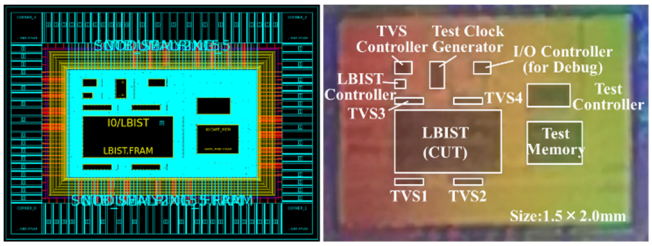
Therefore, by correcting the temperature and voltage influences for the measured delay using the polynomial approximation, it is possible to measure the delay increase due to aging as with the linear approximation.

IV. Evaluation with Test Chip

A. Test Chip Architecture

In order to verify the feasibility of the path delay measurement with correction for temperature and voltage variations, a test chip is designed. The test chip is designed with 65 nm CMOS technology, the core voltage is 1.20 V, the chip size is 1.5 x 2.0 mm. Figure 4 and Table I show a test chip architecture and main functions mounted on the chip, respectively. The CUT (Circuit Under Test) is the OR1200 core of OpenCores minSoC [26]. Then, typical logic BIST is constructed to the CUT. The variable test clock generator is designed based on a method using delay difference between multiple delay elements as explained in the next subsection. Four temperature and voltage sensors (TVSs) are mounted on the chip. The test controller that manages an entire test architecture, an internal memory used to store test conditions or results, and an I/O controller are also mounted.

In order to perform the temperature and voltage evaluation for the chip, a thermostatic bath (SU-241, ESPEC Corp.) and a tester (CX1000D, Advantest Corp.) were used. The thermostatic bath controls the chip temperature, and the tester controls supply voltage, chip operation, and input clock speed.



(a) Chip layout (b) Fabricated test chip

Figure 4. Test chip with 65 nm CMOS technology (1.5 x 2.0 mm)

TABLE I. Main Functions Mounted on the Test Chip

Module	#Gates	Description	Note
Test Controller	8.2k	Controller of entire test architecture	-
Test Internal Memory	21.0k	Storage of test condition and result	-
Test Clock Generator	1.0k	Generation of variable test clock	-
TVS Controller	1.1k	Controller of RO oscillation	-
TVS	1.5k	Temperature and voltage sensor	3 ROs x 4 Units
Logic BIST (CUT, TPG, RA, ets.)	69.6k	Logic BIST architecture	CUT is minSoC

B. Variable Test Clock Generator for Delay Measurement

Figure 5 shows a variable delay path in the variable test clock generator. Two output clocks are used as a capture and launch signals in logic BIST, respectively. The variable delay path consists of buffer chains, the number of the buffers through which the clock passes can be controlled by a parameter *DLYC*. When the *DLYC* is set, the output clock delayed according to the delay amount corresponding to the *DLYC*. The *DLYC* can delay the *TCLK_L* that used as the launch signal, the interval between launch and capture signals can be shortened. Since the test timing becomes smaller by shortening the interval, it suggests that the test clock become faster.

An evaluation using SPICE simulation with 65nm CMOS technology is performed for the designed variable test clock generator. Table II shows the evaluation results of a resolution of the variable test clock generator. The amount of delay of one buffer corresponding to one count in the *DLYC* can be known from the amount of delay increase when the *DLYC* is changed. Its resolution is 23.60 ps under 60 °C and 1.20 V. Also, in the temperature range of 30 to 80 °C and the voltage range of 1.05 to 1.35 V, it was confirmed that its variation of resolution is range of 22.28 to 33.75 ps.

Furthermore, an evaluation using an actual test chip is performed for the variable test clock generator. The resolution can be measured from a pass/fail boundary of logic BIST when changing an input clock speed sequentially. The delay of one buffer, which is the resolution of the variable clock generator, is 26.30 ps. it was confirmed that the value is very close to the evaluated result of simulation.

In Table II, when the number of buffers is 127 (*DLYC* is "01111111"), the delay amount is 3017.31 ps. However, when the number of buffers is switched to 128 (*DLYC* is "10000000"), the delay amount reduced 2999.02 ps. This is a phenomenon due to a layout structure of the designed variable delay path of the variable clock generator. Figure 6 shows the layout structure of the variable delay path. The placement of buffer logic gates and its wire routing differ between a total 127 buffers that the structure of *DLYC*[0, 1, 2, …, 6], and a total 128 buffers that the structure of *DLYC*[7]. When the layout is different, the delay of each buffer path is not the same because of an influence of process variations for wiring delay or gate delay. Thus, it is considered that the total delay value was reduced when *DLYC* was switched "01111111" to "10000000".

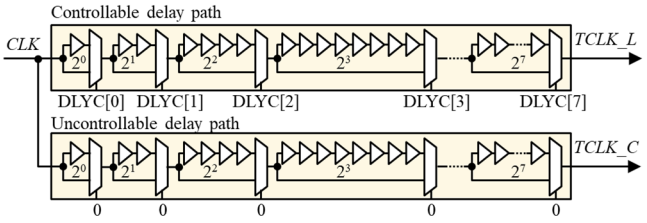


Figure 5. Variable delay paths in the variable test clock generator.

TABLE II. Evaluation of Variable Delay Path by Simulation

DLYC	#Buffer	Delay [ps]	DLYC	#Buffer	Delay [ps]
00000000	0	-	01111111	127	3017.31
00000001	1	20.93	10000000	128	2999.02
00000010	2	46.65	10000001	129	3021.17
00000011	3	68.35	10000010	130	3044.47
00000100	4	92.40	10000100	132	3091.70
00000101	5	115.52	10001000	136	3186.43
00000110	6	138.80	10010000	144	3377.75
00000111	7	160.88	10100000	160	3757.92
00001000	8	187.43	11000000	192	4531,78
00001111	15	348.31	11111101	253	5972.08
00010000	16	378.43	11111110	254	5995.40
00011111	31	726.02	11111111	255	6017.02
00100000	32	758.70			
00111111	63	1484.64	Average of one buffer 23.60		
01000000	64	1532.25			

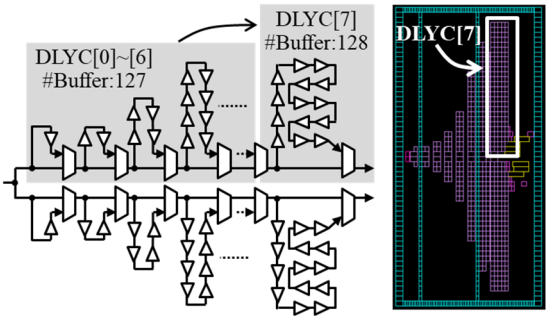


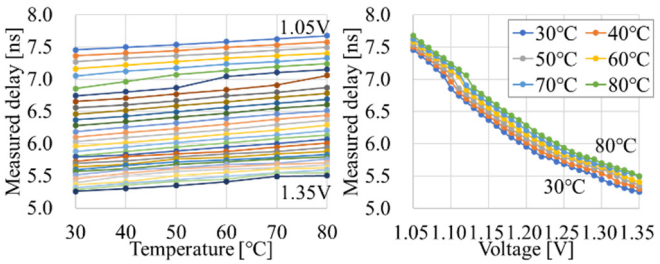
Figure 6. Architecture of variable delay paths.

C. Temperature and Voltage Variation of a Delay

An evaluation of temperature and voltage influences for the test chip, which has the designed delay measurement circuit is performed. Since a SPICE simulation of the entire CUT with varying temperature and voltage is very time consuming, circuit characteristics were evaluated in advance using the test chip in this experiment. The resolution of the variable clock to be used for the delay measurement is 23.60 ps that obtained using simulation evaluation in (60 °C, 1.20 V). The temperature and voltage conditions applied to the chip are 30 to 80 °C (10 °C steps) and 1.05 to 1.35 V (0.01 V steps), respectively.

Figure 7 shows the relation between the measured delay, temperature, and voltage using the test chip. Figure 7(a) and Figure 7(b) show the temperature characteristic and the voltage characteristic for the delay, respectively. It was confirmed that the delay increases when the temperature increases, and the delay decreases when the voltage increases. Also, it was confirmed that the temperature characteristic shown in Figure 7(a) has high linearity, whereas the voltage characteristic shown in Figure 7(b) has weak linearity. There is a variation around 7.0ns measurement delay value. This is because the decrease in the delay value of the variable test clock generator when the *DLYC* switches from "01111111" to "10000000" that described in the previous section.

From the measured results, it was confirmed that delay measurement is possible with the variable clock resolution of 23.60 ps. In 60 °C and 1.20 V, which is assumed to be the initial measurement in the field, the measurement delay value D_0 is 6149.10 ps. In the range of 30 to 80 °C and 1.05 to 1.35 V, the maximum value of the delay is 7768.14 ps (D_0 + 1529.04 ps), the minimum value is 5259.53 ps (D_0 −889.57 ps), the range of delay variation is 2418.61 ps.



(a) Temperature characteristic (b) Voltage characteristic

Figure 7. Relation among the measured delay, the tempterature, and the voltage in the delay measurement.

D. Evaluation of Correction using Linear Approximation

The proposed correction method of temperature and voltage influence for the delay with linear approximation is evaluated. A linear correction equation for the temperature and voltage influence is derived from the measured delay value, temperature and voltage shown in Figure 7 using multiple regression analysis. The derived linear correction equation and the corresponding coefficients are shown in equation (15) and Table III (a).

$$D_{Corrected} = D_{Measured} - \{\alpha_1(T - T_0)\} - \{\beta_1(V - V_0)\} \quad (15)$$

Where, T_0, V_0, D_0 are the temperature and voltage in the initial measurement and the measurement delay value at that time. $D_{Measured}$ is the measured delay and $D_{Corrected}$ is the corrected delay that corrected the temperature and voltage influences from the $D_{Measured}$. α_1 and β_1 are the temperature coefficient and the voltage coefficient for the delay for the linear correction equation, respectively. T and V are the on-chip temperature and voltage at the time of delay measurement. In this evaluation experiment, the set values of the experimental equipment are used. Note that, when actually performing the correction process in the field, the measurement values by the on-chip temperature and voltage sensors are used.

Figure 8 shows the corrected delay values that corrected the temperature and voltage influence using the linear correction. In the range of 30 to 80 °C and 1.05 to 1.35V, the maximum value of the delay is 6557.60 ps (D_0 +408.50 ps), the minimum value is 6144.27 ps (D_0 −4.83 ps), the range of delay variation is 413.33 ps. It was confirmed that the amount of delay variation 2418.61 ps without correction can be reduced to 413.33 ps using the linear correction. Figure 8(b) shows the voltage characteristic of after correction. Since a simple linear correction was used, it was confirmed that the error increased as the measurement point moved away from (60 °C, 1.20 V). The result is suggested that the curve of the voltage characteristic could not be corrected because of the linear correction.

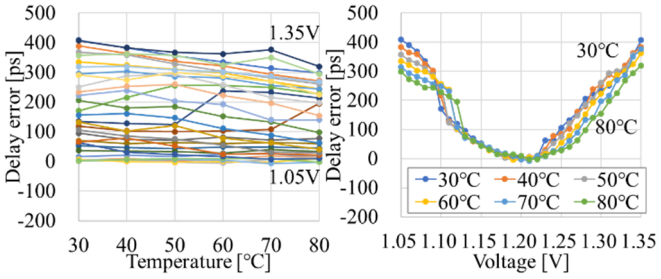
TABLE III. SETTING PARAMETER AND CORRESPONDING COEFFICIENTS

(a) Linear approximation

Parameter	Unit	Value	
T_0	°C	60	Pre-setting values
V_0	V	1.20	
D_0	ps	6149.10	
T	°C	-	Measured values for each chip in the field
V	V	-	
$D_{Measured}$	ps	-	
α_1	ps/°C	6.595	Coefficients for all chips
β_1	ps/mV	-7.326	

(b) Polynomial approximation

Parameter	Unit	Value
T_0	°C	60
V_0	V	1.20
D_0	ps	6149.10
T	°C	-
V	V	-
$D_{Measured}$	ps	-
α_1	ps/°C	6.768
α_2	ps/°C²	0.012
β_1	ps/mV	-7.326
β_2	ps/mV²	18.310



(a) Temperature characteristic (b) Voltage characteristic

Figure 8. Evaluation of correction using linear approximation.

E. Evaluation of Correction using Polynomial Approximation

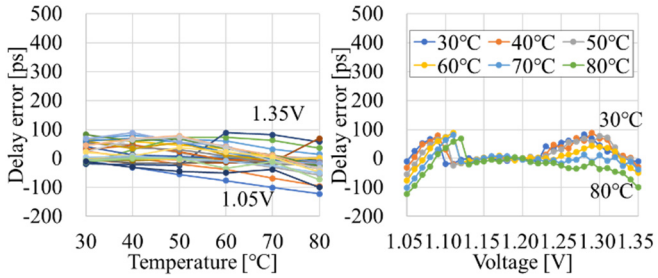
The proposed correction method of temperature and voltage influence for the delay with polynomial approximation is evaluated. As with the linear correction equation, a polynomial correction equation for the temperature and voltage influence is derived from the measured delay value, temperature and voltage using multiple regression analysis. The derived quadratic polynomial correction equation and the corresponding coefficients are shown in equation (16) and Table III (b).

$$D_{Corrected} = D_{Measured} - \{\alpha_1(T - T_0) + \alpha_2(T - T_0)^2\} - \{\beta_1(V - V_0) + \beta_2(V - V_0)^2\} \quad (16)$$

Where, $\alpha_1, \alpha_2, \beta_1$, and β_2 are the temperature and voltage coefficient for the polynomial correction equation, respectively. In this evaluation, since the temperature characteristic has high linearity, it was confirmed that the coefficient α_2 of the quadratic of temperature is close to 0.

Figure 9 shows the corrected delay using the polynomial correction. In the range of 30 to 80 °C and 1.05 to 1.35 V, the maximum value of the delay is 6238.47 ps (D_0 +89.37 ps), the minimum value is 6027.01 ps (D_0 −122.09 ps), the range of delay variation is 211.46 ps. It was confirmed that the amount of delay variation 2418.61 ps without correction can be reduced to 211.46 ps using the polynomial correction.

Table IV shows the amount of delay variation before correction of temperature and voltage influence, the corrected delay using the linear correction, and that of using the polynomial correction. The delay variation 2418.61 ps without correction was reduced to 413.33 ps using the linear correction and to 211.46 ps using the polynomial correction. It was confirmed that the delay variation could be further reduced using the polynomial correction, compared to using the linear correction. Therefore, it suggests that the proposed method can realize a delay measurement independently of temperature and voltage during testing, and it can detect the delay increase due to aging.



(a) Temperature characteristic (b) Voltage characteristic

Figure 9. Evaluation of correction using polynomial approximation.

TABLE IV. COMPARISON BETWEEN THE CORRECTION METHODS

Delay [*ps*]	Before correction	Correction with linear	Correction with polynomial
Initial (60°C, 1.20V)	6149.10	6149.10	6149.10
Max.	7678.14 (+1529.04) at (80°C, 1.05V)	6557.60 (+408.50) at (30°C,1.35V)	6238.47 (+89.37) at (40°C,1.29V)
Min.	5259.53 (-889.57) at (30°C, 1.35V)	6144.27 (-4.83) at (60°C,1.19V)	6027.01 (-122.09) at (80°C,1.05V)
Range	2418.61	413.33	211.46

V. CONCLUSIONS

This paper proposed a method to correct a delay that is varied due to influence of temperature and voltage variation in field using temperature and voltage values that can be measured by such as an on-chip sensor. The method analyzes temperature and voltage characteristics of a circuit delay in advance, and the characteristics are expressed as a polynomial approximation for correction processing. In evaluation using a test chip with 65nm CMOS technology, it was confirmed that a variation of the measured delay can be reduced from 2418.61 to 211.46 ps in the ranges of 30 to 80 °C and 1.05 to 1.35 V. Therefore, the delay measurement independently of on-chip temperature and voltage during testing can be realized using the proposed method. It is useful for detection of the delay increase due to aging.

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