DUT Temperature Coefficient and Power Cycles to Failure

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***Abstract*— We demonstrated power cycling tests with different temperature coefficient samples and shown that cycles to failure strongly depends upon the coefficient. The test samples are investigated by SAT before and after the failure. As a result, we clarified the relationship between the DUT temperature coefficient and failure mechanism. The temperature coefficient is extremely important as a parameter for power cycle tests. High temperature coefficient can lead shorter cycles to failure by thermal runaway before bonding wire disconnection. We also proposed a new method to control temperature coefficient of DUT with gate voltage clamping to drain voltage.**

Keywords— Power cycling test, Temperature Coefficient, SAT, Thermal Runaway, Solder Crack

I. INTRODUCTION

Power cycling test is one of the standard test for predicting device life time[1]. The test results are used as feedback to the package design and basic data of the package life time prediction. During the power cycling test, DUT is heated up by loss generated in the chip inside the package.

Recently, power cycles to failure of power MOSFTs depends up on the method of the chip loss generation. For example, the power cycle to failure with body diode loss generation was match shorter than that for MOSFET switching loss and conduction loss[2][3]. This difference has been explained by the current crowding at wire bonded due to the influence of temperature coefficient[4].

However, power cycles and temperature coefficients of DUT has not been clearly analyzed based on experiments. It is required to clarify the effect of the temperature coefficient in order to improve the accuracy of the power cycle test.

In this paper, we demonstrated power cycling test with different temperature coefficient samples and shown that cycles to failure strongly depends up on the coefficient.

II. TEST SYSTEM CONSIDERING TEMPERATURE COEFFICIENT

In this study, we proposed a new power cycling test method that takes the temperature coefficient into consideration.

A. Stress application and temperatuer coefficient control

In the experiment, a 40V 195A rated power MOSFET was used as the DUT, and the loss caused by heating the DUT was the forward conduction loss of the MOSFET. The DUT used has the characteristic that the drain current value rises as the junction temperature rises (positive temperature dependence). In general, silicon power device V_{th} shift with temperature is negative value of dV_{th} / dT = -5~10mV/K.

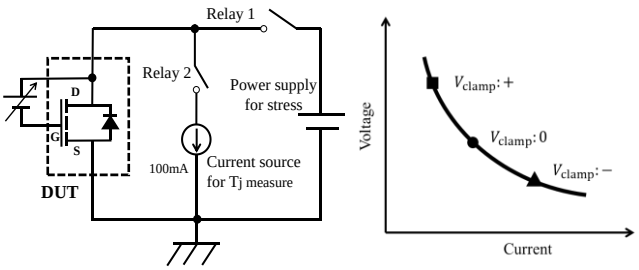

Fig. 1 Test circuit and temperature coefficient

That is, the temperature coefficient becomes large in the small current region where the gate voltage is low. While high current region, coefficient becomes smaller or negative with decrees of electron mobility.

The gate terminal and drain terminal of the DUT were connected via a voltage source (V_{clamp}) as shown in Fig. 1. The temperature coefficient can be controlled by V_{clamp} value. The bias voltage V_{clamp} adjusts voltage drop in the MOSFET and conduction current was controlled so that the generated heat was equivalent for all samples (see Fig. 1). The higher the voltage value of the V_{clamp}, the higher the temperature coefficient. Conversely, the voltage value of the V_{clamp} is set small or negative, the temperature coefficient will be low.

B. Cooling method

Fig. 2 shows how to cool the DUT. The DUT was water-cooled by a heat sink via a metal cylinder for adjusting thermal resistance and a DBC substrate (AlN) for insulation. We used brass cylinders as the metal cylinder material. Water at a constant temperature was flowed through the water-cooled heat sink using a 1200 W chiller.

Thermal grease was applied to the joints between the DUT and the metal cylinder, the metal cylinder and the DBC base, and the DBC base and the water-cooled heat sink. The same amount of heat conductive grease was applied under all conditions so as not to change the thermal resistance value under each condition.

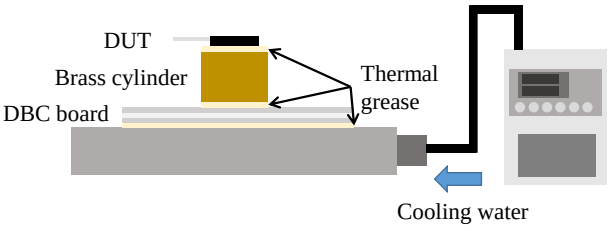

Fig. 2 Cooling method

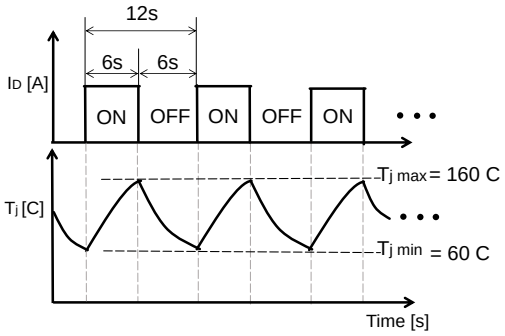

Fig. 3 Test sequence

C. Test Sequence

The test sequence is shown in Figure 3. The test time was 12s for one cycle with an on time of 6s and an off time of 6s. The temperature conditions were such that the junction temperature was 60℃ to 160℃ and the temperature difference was 100℃. The junction temperature was measured from the temperature dependence of forward characteristics of the DUT body diode[5][6].

The temperature characteristics are affected by the stress power supply by putting the DUT in a constant temperature bath in advance and using a relay using the value measured using a curve tracer to instantly switch between the stress power supply and the sense power supply. It is possible to measure the junction temperature without any problems.

III. Test Rezult

The power cycle test was performed under four conditions (Case A, Case B, Case C, Case D) with different temperature coefficients by adjusting the applied voltage of V_{clamp}(see Fig 4). The V_{clamp} values were -1.26V for Case A, 0V for Case B, 3.0V for Case C, and 5.6V for Case D, in ascending order of temperature coefficient. In Case B, since the value of V_{clamp} is set to 0V, the power cycle test was conducted as a 2-terminal element by directly connecting the gate terminal and drain terminal without inserting a power supply.

As for the stress application conditions, the applied power was set to almost the same value (about 300 W), and the ratios of drain current and drain-source voltage were adjusted according to the respective temperature coefficient conditions (see Fig. 5). The values of drain current and drain-source voltage under each condition were 78.2A and 3.8V for Case A, 62A and 4.8V for Case B, 40A and 7.6V for Case C, and 30A and 9.8V for Case D.

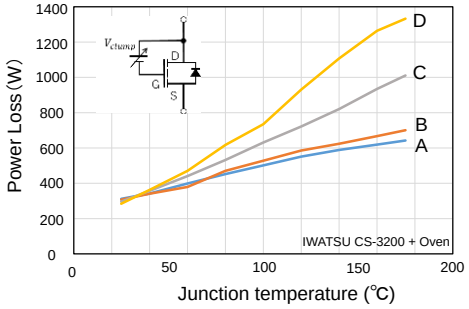

Fig. 4 Temperature dependence of conduction loss generation for DUT samples

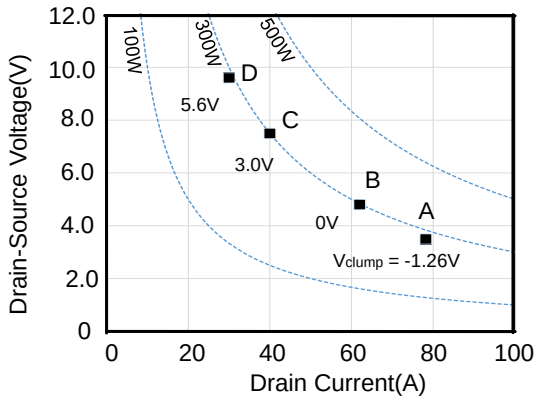

Fig. 5 Conduction loss generation condition of DUT samples

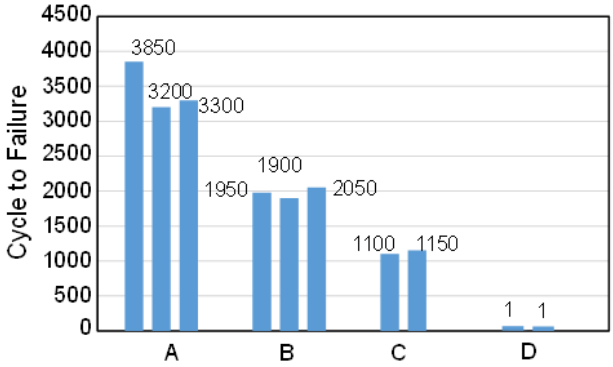

Fig. 6 Cycles to failure for DUT samples of different temperature coefficients, Case A, B, C and D

A power cycle test was conducted with 3 samples of Case A, 3 samples of Case B, 2 samples of Case C, and 2 samples of Case D, for a total of 10 samples. The test results are shown in Fig. 6. In ascending order of the number of cycles until failure, Case D had 1 cycle, Case C had about 1100 cycles, Case C had about 2000 cycles, and Case A had 3200 cycles or more. Case D was able to obtain the same results in the two samples. According to the results, Case A, which has the smallest temperature coefficient, has a longer number of cycles to failure, and Case D, which has the largest temperature coefficient, has a shorter number of cycles. It was also found that the number of cycles until failure decreases as the temperature coefficient increases.

A. Changes in Electrical Characteristics

Fig. 7 shows a graph of changes in electrical characteristics of Case A, Case B, and Case C. A graph was created by plotting the voltage value every 50 cycles leading up to the failure. The vertical axis is the rate of increase from the initial drain-source voltage, and the horizontal axis is the number of cycles. Case D failed in one cycle, so it was not possible to capture changes in electrical characteristics. From the graph, it can be confirmed that there is a difference in the change in electrical characteristics between Case A, Case B, and Case C.

In Case A, it can be confirmed that the drain-source voltage gradually increases as the number of cycles increases. In addition, it is considered that the voltage rises sharply around 3000 cycles and 3500 cycles because the bonding

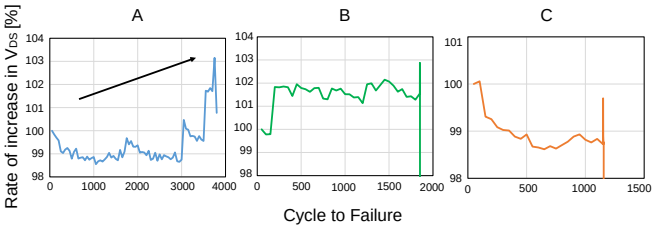

Fig. 7 V_{DS} voltage changes during the power cycling test in case A, B and C

wire is lifted off. In Case B, the voltage change leading up to the failure was small, and the voltage rose immediately before the failure, leading to the failure. In Case C, the voltage gradually dropped from the initial value, and the voltage rose just before the failure, leading to the failure.

The voltage rise rate at the time of failure is 99.1% for Case A, while it decreases to 40% or less for Case B and Case C. It is possible that there is a difference in the failure mechanism due to the difference in temperature coefficient.

B. Internal Structural Change

Fig. 8 shows the SAT (Scanning Acoustic Tomography) images before and after the power cycle test for each condition. The SAT image is the observation result of the interface between the bonding wire and the chip. The upper row is the image before the power cycle test, and the lower row is the image acquired after the failure of each case.

From the result of Fig. 8, the white broken line is considered to be the failure mark in each case. In Case B, failure marks appear linearly from the lower right of the chip to the center of the chip. In Case C, a failure mark can be confirmed at the same position as Case B, but unlike Case B, the failure mark does not extend to the center of the chip. In Case B and Case C, it was found that a failure mark was formed in the part where the retreat of the solder layer was large. In Case D, a spot failure mark different from Case C and Case B can be confirmed in the center of the chip.

Focusing on the bonding wire, Case A makes the connection surface of the bonding wire unclear compared to other conditions. The cause of the failure in Case A is thought to be the lift-off of the bonding wire. Further, it can be seen that there is a large difference in the peeled area of the solder layer depending on each temperature coefficient. The peeled part is the lower part of the chip at all temperature coefficients.

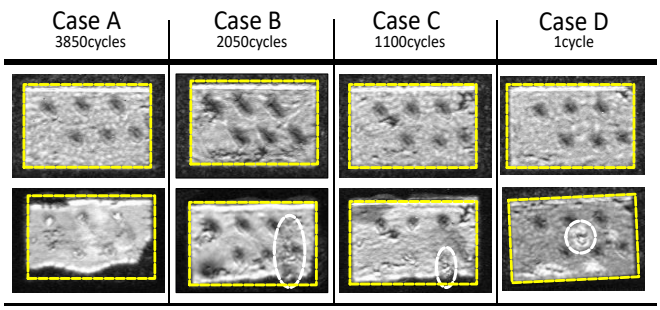

Fig. 8 SAT images of failed samples of Case A, B, C and D (Temperature coefficient A < B < C < D)

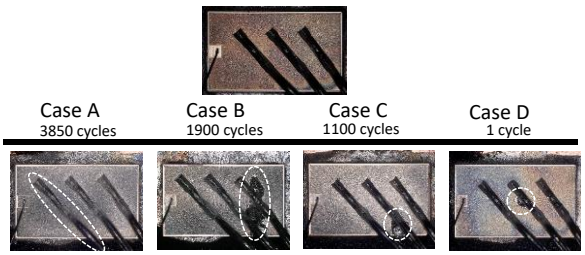

Fig. 9 Top images of failed samples of Case A, B, C and D (Temperature coefficient A < B < C < D)

This is because the lower part of the chip is close to the drain, source, and gate terminals of the device, so the temperature tends to rise. The SAT image was binarized and the peeled area was calculated. Case A was 18.5%, Case B was 9.8%, Case C was 9.6%, and Case D was 5.2%. Case A with the lowest temperature coefficient (longer number of cycles to failure) has the largest peeling area, and Case D with the highest temperature coefficient (shorter number of cycles to failure) has the smallest peeling area. It was.

C. Chip Surface Changes

After the power cycle test, the mold resin was melted and the surface of the chip was observed with a microscope. Figure 9 shows micrographs in each case. In Case A, it was found that the bonding wire in the white dashed line was damaged. In Case B and Case C, you can see a black mark on the lower right of the chip that looks like the device has melted. In Case B, it can be seen that the melted part extends to the upper part of the chip. In Case D, the type of failure mark is the same as Case B and Case C, but the location of occurrence is in the center of the chip.

Comparing with the SAT image, it was confirmed that the chip surface was faulty because there were fault marks in the same place and in the same range.

IV. Discussion of Failure Mechanism

Fig. 4 In Case D, when stress is applied and the junction temperature rises to 160 °C, a chip loss of 1200 W or more occurs. Since the device's cooling capacity has been significantly exceeded, a failure due to thermal runaway is suspected. Further, since the failure mark is generated only on the central bonding wire and the ground plane of the chip, it is considered that the current is concentrated. Fig. 10 shows a model of the effect of the temperature coefficient on the failure mechanism. In Case B and Case C, a failure mark appears from the receding part of the solder layer, and in Case B, the failure mark extends to the central part along the bonding wire.

As stress is applied and the number of cycles increases, the peeling of the solder layer gradually progresses. At the peeled portion of the solder layer, the value of thermal resistance gradually increases compared to the initial value. As the thermal resistance increases, the heat dissipation capacity of the device gradually deteriorates. When the heat dissipation capacity drops to a certain amount, the power loss of the chip exceeds the heat dissipation capacity and the chip cooling becomes insufficient. As a result, thermal runaway occurs.

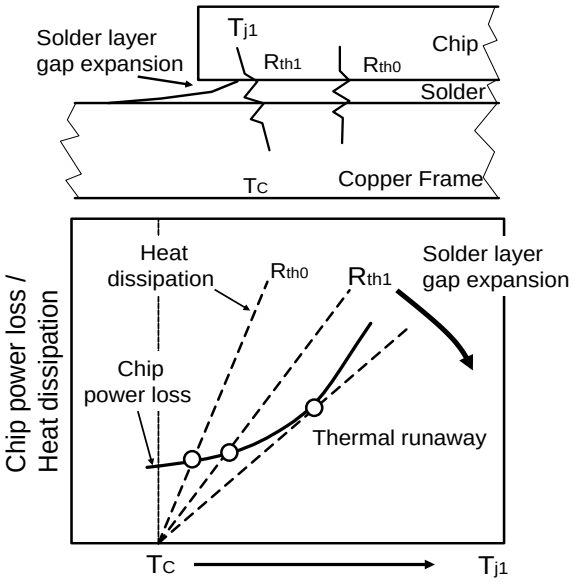

Fig. 10 Model diagram of the effect of temperature coefficient on failure mechanism

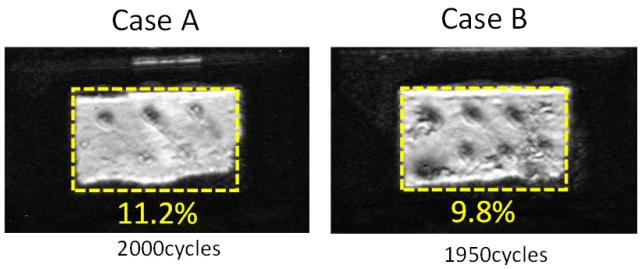

Fig. 11 Comparison of SAT images around 2000 cycles of Case A and Case B

In both Case B and Case C, the lower right part of the device (near the bonding wire in the center) has a large retreat of the solder layer peeling, and failure marks also appear in the peeling retreat part.

From this, it is conceivable that the central bonding wire has a current flowing through it (current concentration is occurring) as compared with other wires. In Case B, it is probable that thermal runaway occurred at the solder retreat in the lower right, and further heat generation was induced by the current concentration, causing thermal runaway to occur in a chain and the failure progressed to the center of the chip.

V. Conclusion

We clarified the relationship between the DUT temperature coefficient and failure mechanism. DUT temperature coefficient strong affect to power cycles to failure. When the power loss of the DUT has large positive temperature coefficient, the failure occurs by solder crack expansion before bonding wire disconnection. On the other hand, when the temperature coefficient is small, the failure occurs by bonding wire disconnection even solder crack expanded to 25% of chip area.

From the above, it was found that it is necessary to take DUT loss generation temperature coefficient into account in power cycling test. High temperature coefficient can lead shorter cycles to failure by thermal runaway before bonding wire disconnection. We also proposed a new method to control temperature coefficient of DUT with gate voltage clamping to drain voltage.

References

[1] Josef Lutz, Heinrich Schlangenotto: “Semiconductor Power Devices”, Springer Berlin Heidelberg, 2011

[2] C. Schwabe, P. Seidel and J. Lutz, “Power cycling capability of silicon low-voltage MOSFETs under different operation conditions” Proc. ISPSD2019, p.495-498(2019) .

[3] G.Zeng, Wenisch-Kober, J.Lutz, "Study on power cycling test with different control strategies”, Microelectronics Reliability, Volumes 88-90, p.p756-761, 2018

[4] C. Schwabe, P. Seidel and J. Lutz, "Simulation of current crowding in inverse diodes of low-voltage Si MOSFETs at power cycling," 21st European Conference on Power Electronics and Applications, pp. 1-7, 2019.

[5] R. Schmidt and U. Scheuermann, "Using the chip as a temperature sensor — The influence of steep lateral temperature gradients on the Vce(T)-measurement," 2009 13th European Conference on Power Electronics and Applications, Barcelona, 2009, pp. 1-9.

[6] Akihiko Watanabe, Masanori Tsukuda, Ichiro Omura,: “Real time degradation monitoring system for high power IGBT module under power cycling test, Microelectronics Reliability”, Microelectronics Reliability, Volume 53, pp. 1692-1696 (2013)

[7] Yuma Kawauchi, Kenji Akimoto, Akihiko Watanabe, Ichiro Omura, “Verification of highly accurate power cycle test method”, Proc. IEEJ ; EDD-20-064,SPC-20-214, in Japanese.