

Calculation of Single Event Burnout failure rate for high voltage devices under satellite orbit without fitting parameters

M. Sudo^a, M. Tsukuda^{b*}, I. Omura^{b*}

^a *Kyushu Institute of Technology, 1-1 Sensui-cho, Tobata-ku, Kitakyushu, Japan*

^b *Kyushu Institute of Technology, 2-4 Hibikino, Wakamatsu-ku, Kitakyushu-shi, , Japan*

Abstract

Increase of power bus voltages in spacecraft are expected with the power demand growth. Accordingly, high voltage semiconductor devices in the power supply system will be required to withstand high energy and high flux cosmic ray environment. In this paper, we propose a new formula to calculate failure rate for power semiconductor devices in space application.

1. Introduction

Weight of power bus wiring reduction of spacecraft, such as satellites or space station, is required for reduced launch costs. In large scale spacecraft, harness mass weight will be a serious problem for the lunch cost. In order to reduce the weight, increase in power bus voltages are required over 300V. The further high power supply voltages are inevitable because the power consumption in space station is predicted to reach to the level of Mega-watt, soon [1].

Introduction of the high power bus voltage in spacecraft raises the serious risk of cosmic ray induced failure due to the high energy proton strike silicon crystal under high electric field. The cosmic ray induced failure in the power devices in the high voltage power supply causes the complete outage of satellite function [2-4]. The failure rate calculation for power semiconductor devices in satellite system becomes an important design issue to introduce the high bus voltage power systems.

Since the cosmic ray induced failure has been discussed only for power semiconductor devices for sea level applications. Thus the terrestrial failure rate had been calculated based on the empirical model extracted from the terrestrial experiment data [5]. Table 1 shows a comparison of proposed method and existing method. The failure rate calculation formula for satellite orbit condition was proposed, for the first time, from our group [6].

However, there are two problems. First,

calculation accuracy was not sufficiently high due to the assumption that the failure phenomenon at high electric field occurs in the entire device with the same probability. Second, since there was only 300 μm -thick silicon data of deposited energy probability, only the failure rate of 300 μm i-layer device could be calculated.

In this paper, we increased the number of TCAD simulation condition, specially, for different the charge deposition position, and propose new formula including the position dependence in the failure rate calculation. The calculation accuracy is improved and new formula become applicable to any breakdown voltage semiconductor devices.

Table 1. Comparison of proposed method and existing method

Method	Pros and Cons
Empirical model by Zeller [3] and after	Simplicity of the formula Extracted from accelerated test Only for an terrestrial condition
Heavy ion irradiation experiments [4]	Efficient for deposited charge based mechanism discussion Sample chip required Difficulty in deposition depth control
High energy neutron/proton irradiation experiments [10, 11]	Accurate if flux specter is reproduced orbit condition Sample chip is required Limited experiment facility
Proposed method[6]	Failure rate for any flux condition Introduction of voltage dependent cross section TCAD simulation required

* Corresponding authors. tsukuda@life.kyutech.ac.jp omura@ele.kyutech.ac.jp

Tel: +81 (93) 695 6037 ; Fax: +81 (93) 695 6037

2. Cosmic ray failure rate calculation method with new formula

2.1. Proposed formula

Cosmic ray induced failure rate is calculated from the integral of the cross section $\sigma(V_{DC}, E_p)$ and the high energy particle flux spectrum $Flux(E_p)$ on the particular orbit (Eq. 1 and Table 2). And the cross section is decomposed into two factors, i.e. newly defined deposited charge probability function in silicon for incident particle per unit length, $\tilde{\Phi}_{E_p}(Q_d)$ and the critical amount of deposited charge to device destruction Q_{dest} .

$$Failure\ Rate(V_{DC}) = \int_{E_{min}}^{\infty} \int_{\Omega} \sigma(V_{DC}, E_p) Flux(E_p) d\Omega dE_p \quad (1)$$

Assuming that cosmic rays come along vertical direction to the chip surface, the formula of failure rate and cross section becomes equation (2) and (3) respectively. 4π represent all solid angles. Deposited charge Q_d was obtained from deposited energy E_d of each strike by assuming a 3.6eV ionization energy for electron-hole pairs [4]. Q_d is equal to integral of the current pulse over a specified period of time in non-avalanche condition.

$$Failure\ Rate(V_{DC}) = \int_{E_p}^{\infty} \sigma(V_{DC}, E_p) 4\pi Flux(E_p) dE_p \quad (2)$$

$$\sigma(V_{DC}, E_p) = A \int_0^l \int_{Q_{dest}(V_{DC}, z)}^{\infty} \tilde{\Phi}_{E_p}(Q_d) dQ_d dz \quad (3)$$

Table 2. Parameter names and units of symbols used in equation (1-3)

Symbol	Parameter name	unit
σ	Cross section	cm^2
$Flux$	high energy particle flux	$MeV^{-1}s^{-1}cm^{-2}sr^{-1}$
E_p	Particle energy	MeV
Ω	Solid angle	sr
A	Device area	cm^2
Q_{dest}	Critical amount of deposited charge to device destruction	C
$\tilde{\Phi}_{E_p}$	Deposited charge probability in silicon	$C^{-1}cm^{-1}$
Q_d	Deposited charge	C
V_{DC}	Applied DC voltage	V
z	Position in depth direction in chip	μm
l	i-layer thickness	μm

2.2.1. Distribution function of high energy particle

The flux observation projects, such as PAMELA, STE-QUEST converted the particle flux distribution into data [7-9]. The proton flux distribution on the orbit was interpolated by combining two observational data.

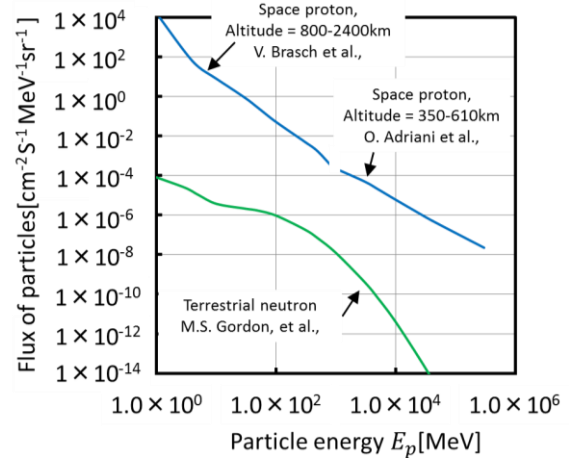


Fig. 2. The terrestrial neutron flux and the space proton flux distribution. Available from reports on the flux observation projects [7-9]

2.2.2. Probability distribution function of deposited charge in silicon by the high energy particle

Figure 3 shows approximate expression for the deposited charge probability function in silicon (300 μm thickness) by the incident particle with reference to the paper [10]. We defined $\tilde{\Phi}_{E_p}(Q_d)$ by the equation (4) because the probability is proportional to the thickness of the device [11].

$$\tilde{\Phi}_{E_p}(Q_d) = \frac{\Phi_{E_p,300}(Q_d)}{300\mu m} \quad (4)$$

Where $\Phi_{E_p,300}(Q_d)$ is probability obtained from Fig.

3.

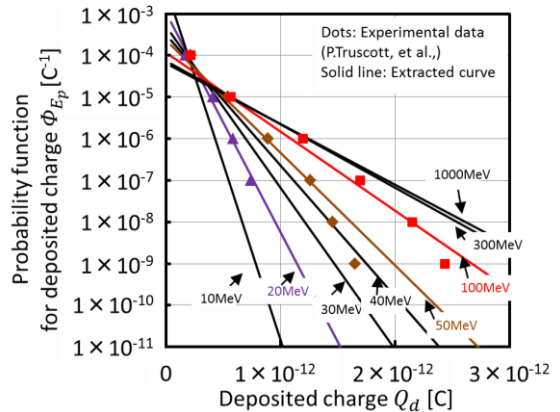


Fig. 3. Deposited charge probability function

in silicon by the incident particle. Available from nuclear science articles [10, 11].

2.2.3. Critical amount of deposited charge to the device destruction

The critical amount of deposited charge to destruction $Q_{dest}(V_{DC}, z)$ is defined as the threshold of deposited charge which cause device destruction. Here, VDC is applied reverse voltage and z is the charge deposit position in depth direction from the silicon surface. We can calculate the cross section by collecting the probability of charge deposition exceed Q_{dest} as shown in Eq. 3. To obtain Q_{dest} for combination of applied voltage VDC and charge deposition position z , a number of TCAD simulations have been carried out. The simulation result will be explained in the next section.

3. Critical amount of deposited charge to the device destruction by TCAD simulation

3.1. Device structure for TCAD

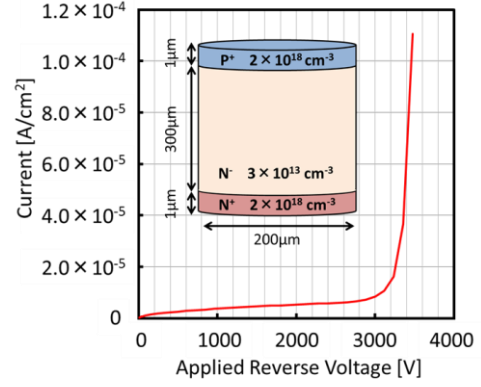
We calculated critical amount of deposited charge to the device destruction Q_{dest} for two types PiN diodes with different breakdown voltage based on TCAD simulation. One structure has 300 μm i-layer and the other has 100 μm i-layer. The device structures and conditions for the simulations are simplified to reduce computation time since obtaining the critical amount of deposited charge to destruction require hundreds of TCAD transient simulations for variety of applied voltage, amount of deposited charge and deposited position.

We assumed cylindrical symmetry for the simulation and deposited charge is placed at the centre of the cylindrical symmetry. We have simulated three different charge deposition depth and extracted the position dependence on the charge generation during the event. The probability of the initial charge deposition by particles is assumed to be uniform along the i-layer depth (z -direction).

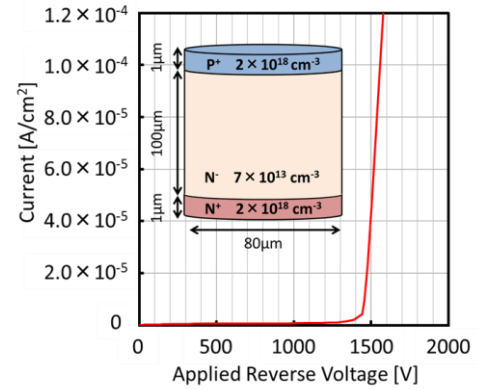
Although the simplification may cause problems on the calculation accuracy because of initial deposited charge (electron-hole pairs) shape in TCAD should be deferent for each event and the shape may need to include the model. In this paper, however, the simplification for TCAD simulation is necessary to obtain the SEB cross section because of the computation time. In section 4.2, the accuracy is confirmed by comparing the empirical formula proposed by Zeller [5] for sea level failure rate and our proposed formulation with the obtained SEB cross section and neutron flux density distribution at sea-level from [7].

In the breakdown simulation results of these device

structures are shown in the figure 4.



(a) 300 μm i-layer PiN diode



(b) 100 μm i-layer PiN diode

Fig. 4. TCAD simulation device structure and reverse bias characteristics.

Figure 5 shows the transient of current density distribution under two different conditions. In lower applied voltage of 1000 V, electron-hole pairs did not induce current filament, and thus the current through the device stops with the extinction of carriers. In higher applied voltage of 2000 V, the current filament continuously appeared due to impact ionization with localized high electric field with the generated charge.

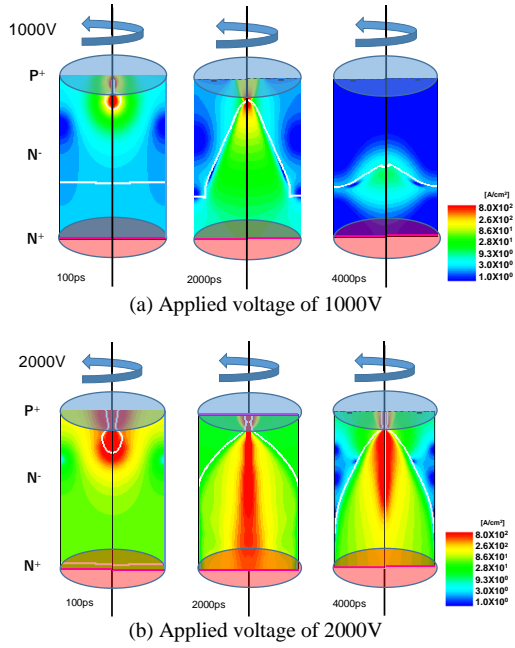
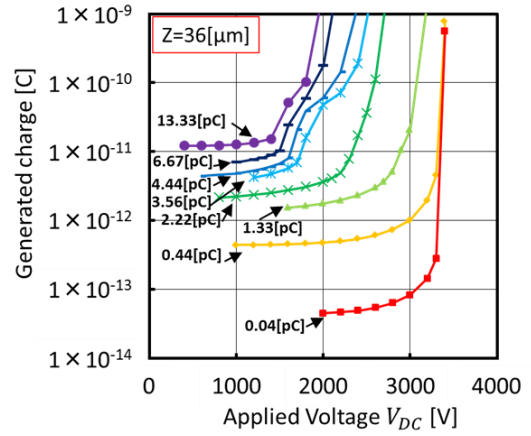


Fig. 5. Total current density distribution after the incident with deposited charge = 6.67pC, $z = 36\mu\text{m}$ for 300 μm i-layer PiN diode. Applied voltages are 1000V (a) and 2000V (b).

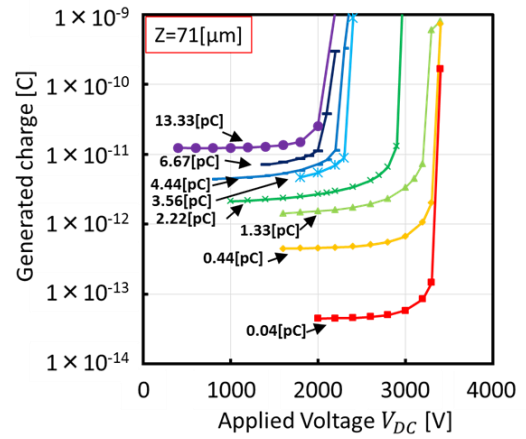
3.2. Calculation results of applied voltage and generated charge

Figure 6 and 7 shows the relationship between applied voltage and generated charge with deposited charge as a parameter for 300 μm and 100 μm i-layer (N^- -layer) length. Generated charge is defined as the integral of the current pulse through the device over a specified period of time of the phenomena.

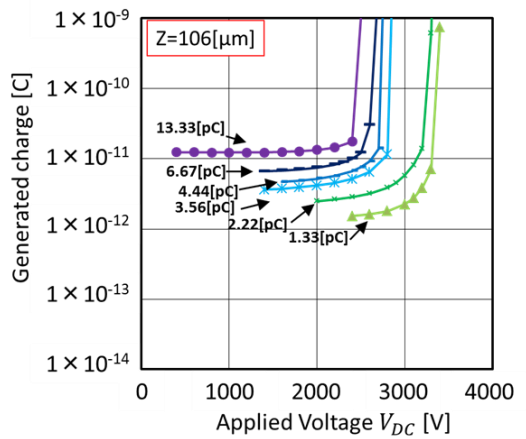
The critical amount of charge to destruction $Q_{\text{dest}}(V_{\text{DC}}, z)$ is extracted from the results shown in Fig. 6 and 7. Figure 8 shows extracted function of Q_{dest} .



(a) Deposited position, $z = 36\mu\text{m}$

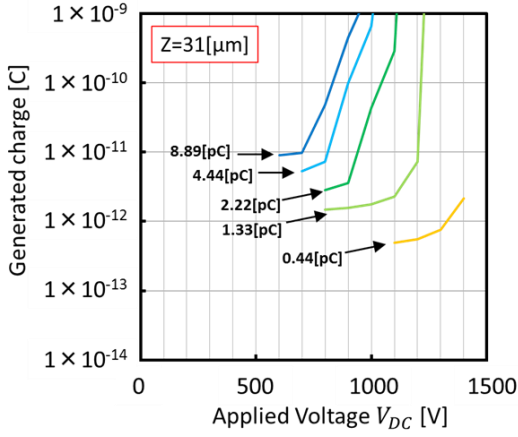


(b) Deposited position, $z = 71\mu\text{m}$

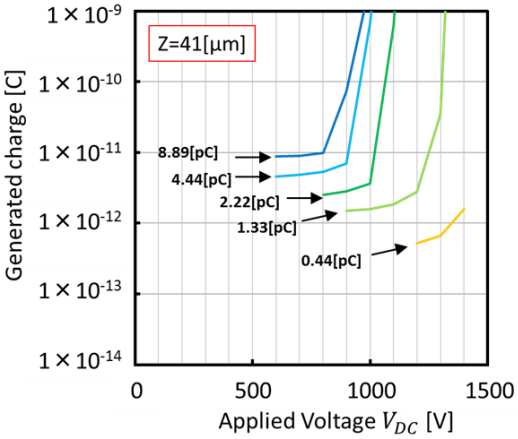


(c) Deposited position, $z = 106\mu\text{m}$

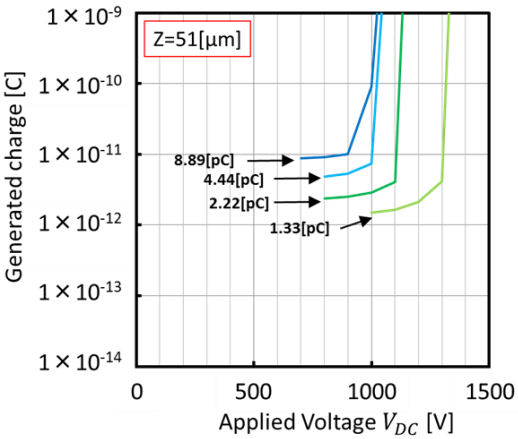
Fig. 6. Relationship between generated charge and applied voltage for different deposited charge (300 μm i-layer PiN diode).



(a) Deposited position, $z = 31\mu\text{m}$

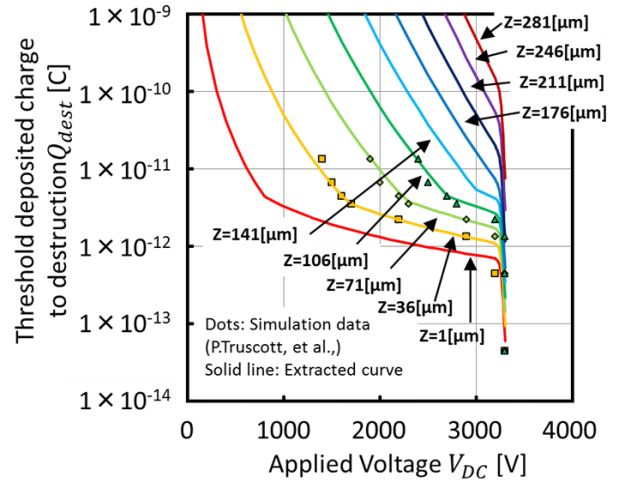


(b) Deposited position, $z = 41\mu\text{m}$

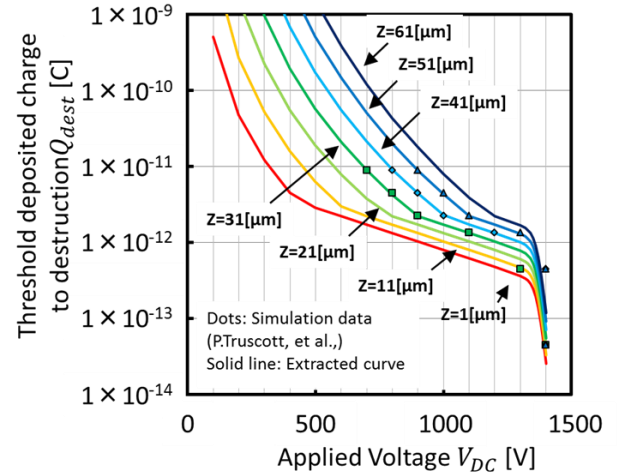


(c) Deposited position, $z = 51\mu\text{m}$

Fig.7. Relationship between generated charge and applied voltage for different deposited charge (100µm i-layer PiN diode).



(a) 300µm i-layer PiN diode



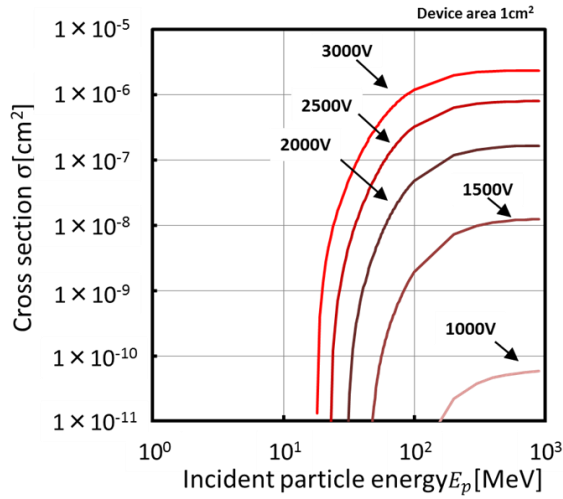
(b) 100µm i-layer PiN diode

Fig. 8. Critical amount of deposited charge destruction. The location of deposited charge is a parameter.

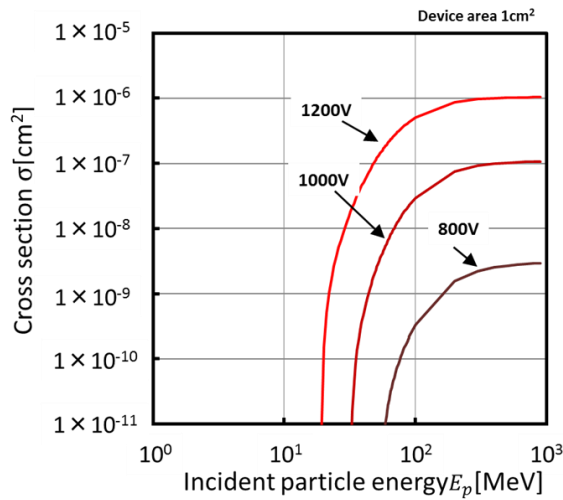
4. Calculation with proposal formulation

4.1. The cross section

The cross section was calculated from the proposed equation (4) and the calculated value of Q_{dest} . Fig. 9 shows the cross section calculation result.



(a) 300 μ m i-layer PiN diode

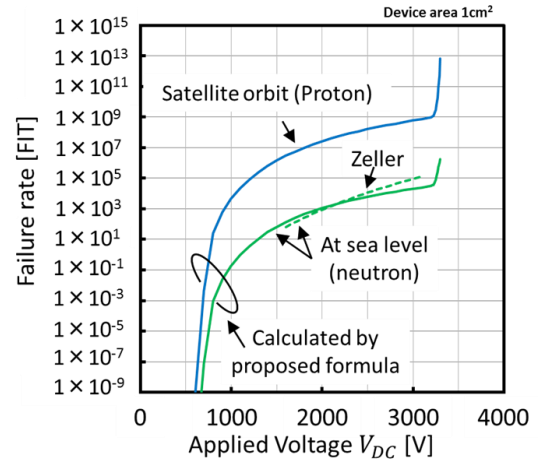


(b) 100 μ m i-layer PiN diode

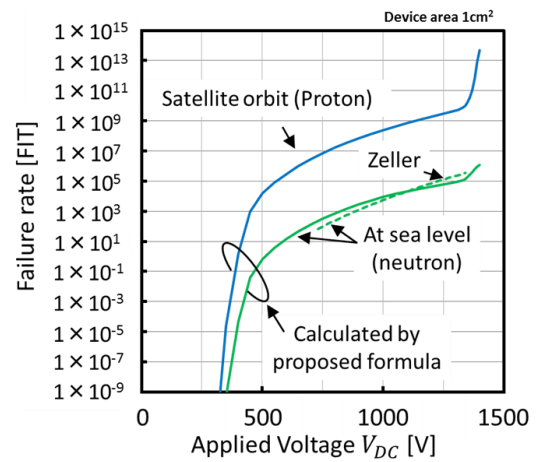
Fig. 9. SEB cross section calculated from the proposed equation and TCAD analysis results

4.2. The failure rate

The failure rate was calculated from the proposed equation (3) and the calculated value of σ . Fig. 10 shows the failure rate calculation result. The failure rate calculation formula is successfully verified by comparing with the failure rate calculated based on acceleration tests on the ground [5].



(a) 300 μ m i-layer PiN diode



(b) 100 μ m i-layer PiN diode

Fig. 10. Failure rate calculated from the proposed equation and TCAD analysis results

5. Conclusion

We proposed a general formulation applicable for any cosmic ray flux conditions, including satellite orbit flux condition. Introducing charge deposition position dependence to the critical charge to destruction and the deposited charge probability function for each incident particle per unit length, failure rate calculation accuracy is improved, which is confirmed with the data at sea level condition.

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