Peak minimization based gate delay compensation for active current balancing of parallel IGBT system

Ravi Nath Tripathi[a,*], M. Tsukuda[b,a], I. Omura[a]

[a] *Kyushu Institute of Technology, Kitakyushu, Fukuoka, Japan*
[b] *Green Electronics Research Institute Kitakyushu (GRIK), Kitakyushu, Fukuoka, Japan*

Abstract

The non-uniform current sharing among the paralleled devices is consequential due to non-identical layout and alteration in parameters of the system consists of power semiconductor devices and gate drivers. The persistent non-uniform current among the paralleled devices arise the various concerns such as de-rating, uneven losses, and heat consequently can lead to reliability and failure issues of the system. This paper presents, a simple yet intelligent and effective automatic control for gate delay compensation to achieve active current balancing through current peak minimization. The current peak minimization control approach can serve the purpose of minimizing system de-rating as well as obtaining nearly uniform dynamic current sharing. The four parallel connected discrete IGBT system is used for experimental validation under unbalanced operating condition. Moreover, the current peak minimization trend evaluation is introduced for gate delay compensation.

1. Introduction

The power electronic converters are the backbone for efficient and reliable electric power conversion. The converters are required with a typical voltage-current rating considering the need for the specific applications. High current power converters are demanded and used for process industries, transport industries and also for the renewable energies [1]. The devices are used in parallel to realize high-current power modules consists of multi-chips inside.

The parallel connection of discrete devices/multi-chip IGBT modules is an appealing choice considering the chip area and maximum possible current capability of a single module for an optimal cost and size of the system [2]. However, the current mismatch among the paralleled system is a major challenge for improving the de-rating and reliability of the entire system [3]. The paralleled discrete devices/multi-chip power module are required to drive through intelligent gate control to minimize the current unbalancing and system de-rating.

The paralleled system characteristics have studied extensively to investigate the behavior of devices and current unbalancing [4]-[6]. The common gate driving unit has used to minimize the effect of uneven gate drive parameters. However, under this scheme, the limitation of a number of parallel connection of modules and unbalancing due to other undesired parameter variation cannot be compensated.

The individual gate driving unit approach is used in [1], [7-10] for compensation of current unbalancing. The compensation control approach is mainly focused on the even current sharing of the paralleled system. However, the even current sharing may possess relatively higher average current peak overshoot that can be defined as overbalancing. The current peak overshoot is crucial to enhance safe-operating-area (SOA) [4], [11-12] issue, as well as, to avoid dynamic overbalancing.

The digital feedback control based on peak minimization concept is presented in [8] to achieve current balancing for paralleled device system. The even current sharing demonstrated for two parallel connected devices under unbalanced turn-on condition. In this work, the current peaks corresponding to two consecutive gate signals are used to ensure current balancing.

In this paper, the automatic delay compensation based on peak current minimization is presented for active current balancing during turn-on and turn-off. Moreover, the novel balancing factor is used for the optimization of current peak minimization considering unit step delay. The automatic gate delay compensation is implemented using a Field Programmable Gate Array (FPGA) for the system consists of four parallel connected discrete IGBT.

* Corresponding author. tripathi_ravi@life.kyutech.ac.jp
Tel: +81 (080) 4319 3555 ;

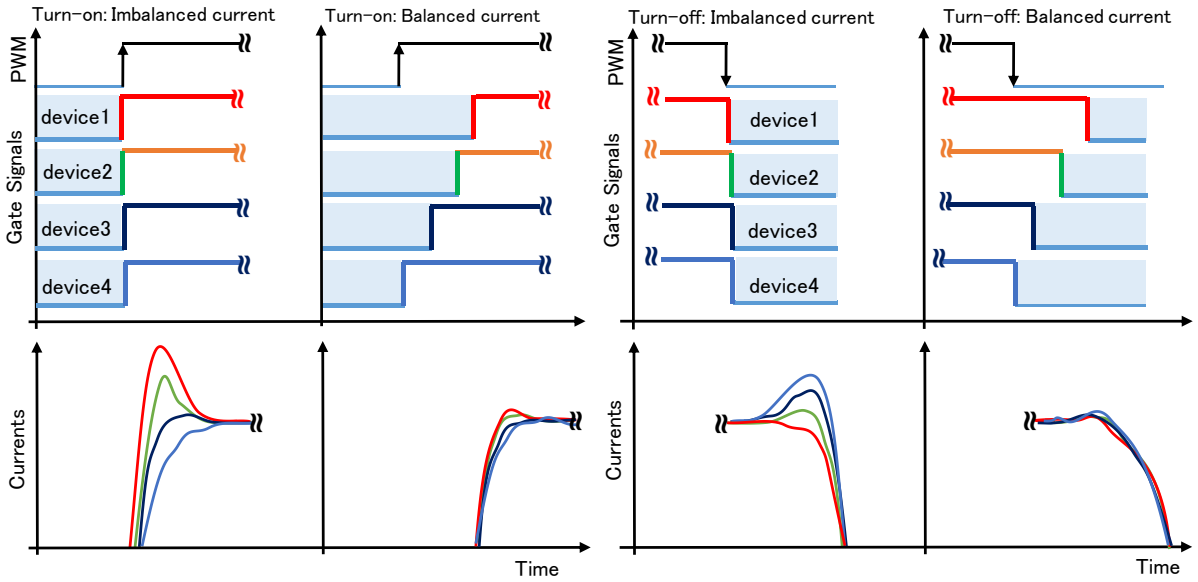

Fig.1 Unbalanced and balanced current conditions corresponding to gate signals for turn-on and turn-off.

2. Gate control for paralleled device system

Gate control for parallel connected power device system is very much mandatory to overcome the fundamental issues associated with the system. The non-identical and asynchronous switching behavior is a source to unbalanced system operation. However, the controlled asynchronous gate signal can be used to minimize the non-identical switching behavior and it will ultimately result in improved system performance and system reliability. The controlled asynchronous gate signal means that the delay time (t_d) adjustment to compensate the current unbalancing (Δi_C) arise due to a mismatch in the paralleled system.

The delay time adjustment techniques were presented in the literature by several authors based upon direct/indirect relation of measured parameters to current mismatch of devices. One of the simplest approach considering the direct relationship between current and delay time $t_d(\Delta i_C)$ is presented in [1]. The rise and fall time control based gate delay adjustment t_d (Δt_r, Δt_f) is implemented in [7-8]. The emitter to auxiliary emitter voltage measurement method used for delay adjustment t_d (Δv_{bond}) [9]. The use of PI controller in [9] to minimize the delay time difference for a system possessing non-linear nature, may easily lead to instability.

Almost all of the methods that can be categorized as either direct or indirect approach are mainly focused on the dynamic current balancing without taking into account the peak current suppression (restraining the peak current). Although, the peak currents are measured in [7], however, it is just used for the monitoring purpose with rise and fall control using quite a complex system implementation method. The approach to obtain active current balancing without peak overshoot control can lead to over-balancing.

The method proposed in [10] is implemented by adopting peak detection and minimization approach for delay control adjustment $t_d(\Delta i_{peak})$. It is also a direct approach for active current balancing. The peak minimization based feedback control approach serving both the requirements dynamic current balancing as well as peak overshoot optimization to avoid over-current balancing.

3. Gate delay compensation control: Methodology

3.1. General

The peak minimization concept based approach in [8] demonstrated the peak minimization as well as even current sharing for two parallel devices through delay time compensation, a simple yet effective way for active current balancing. In this paper, the gate delay control method is further improved by using simplified balancing factor and easily possible to expand to several numbers of devices. In addition, this approach can be applied to direct/indirect gate delay compensation method however direct compensation method does not require extraction of delay information like in indirect approach of active current balancing method.

This gate delay compensation method can be summarized in the following points:

1. Measurement of the control parameter (in this

case IGBT current)

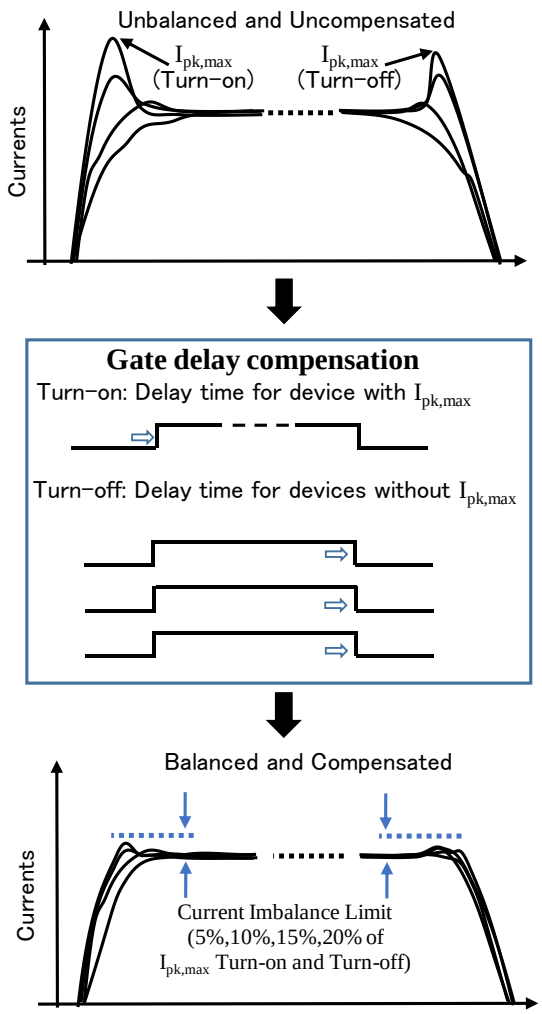

Fig.2 Gate delay compensation control bases on the maximum current peak.

2. Peak detection (Turn-on and Turn-off)
3. Independent unit delay adjustment in gate signal for turn-on and turn-off

The following are the advantages for industrial application summarized as follows:

1. Set the current imbalance limit corresponding to the unit delay time.
2. Implementation flexibility for low cost (fully digital or analog-digital hybrid).
3. Independent turn-on and turn-off control.
4. Not affected by the delay in signal measurement.

3.2. Delay compensation

The fundamental point that needed to take care of the system, is over-compensation to avoid undesired current overshoot and swing that can easily lead to

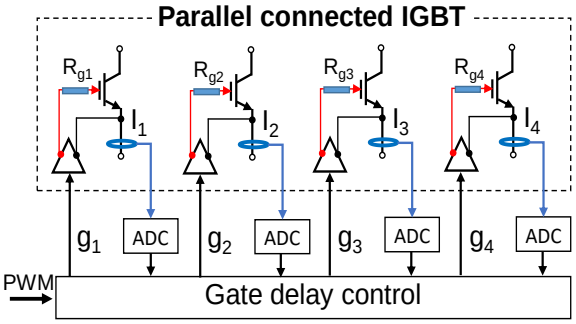

Fig.3 Schematic representation of parallel connected IGBT system for experimental validation.

instability. The effect of change of parameters such as junction temperature and system aging etc. are possessing significantly slow time constant (few seconds or minutes) [9] as compared to system dynamic in hundreds of ns/µs.

The unit delay compensation is adopted for active
current balancing to avoid the foremost possibility of over-compensation. In addition, the unit delay time is
need to be chosen moderately to maintain significant dynamic response for balancing control.

3.2.1 Enabling delay control:

The delay control is enabled based upon the dynamic maximum current peak overshoot ($I_{pk,max}$) imbalance and current imbalance limit. The peak currents ($I_{pk,j}$) of 'n' parallel connected devices, are detected individually and further $I_{pk,max}$ is computed.

$$I_{pk,max}^{on} = max\{I_{pk,j}\};\ (j = 1, \dots, n)$$

$$I_{pk,max}^{off} = max\{I_{pk,j}\};\ (j = 1, \dots, n)$$

The balancing factor (b.f.) is computed using the current imbalance limit, and compared with current peaks $I_{pk,j}$. If the current imbalance limit set to10% of the $I_{pk,max}$ the b.f. is defined as

$$\text{b.f.} = 0.9 * I_{pk,max}$$

If the peak current of other devices falls inside b.f. then the delay control will not be enabled. For the case of peak current unbalancing more than 10% considering turn-on and turn-off both the cases, the delay control is enabled to minimize the peak and achieve the current peak within the desired range.

3.2.2 Delay adjustment:

Delay compensation control is enabled for unbalancing and gate signal delays are adjusted

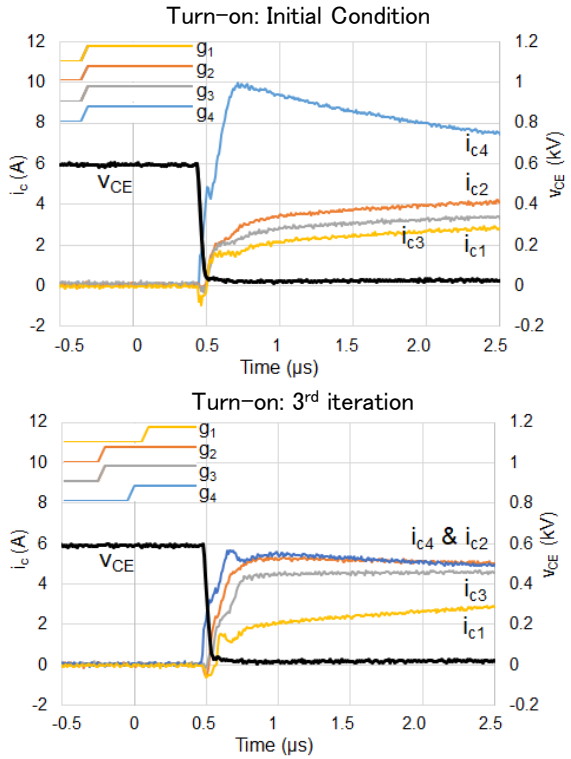

Fig.4a Measured IGBT currents for four parallel connected IGBTs during turn-on.

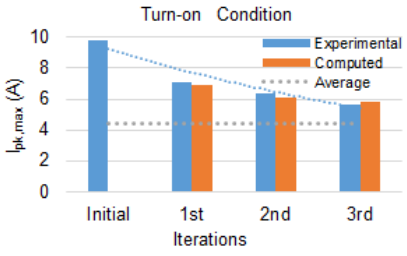

Fig.5a Maximum peak current minimization trend during turn-on condition.

correspondingly based upon their peak current. Suppose i^{th} and k^{th} IGBT possessing $I_{pk,max}$ during turn-on and turn-off respectively for N^{th} PWM pulse, therefore, the delay time is compensated for next PWM sequence as:

Turn-on condition:

$$t_{d,j}^{on}(N+1) = \begin{Bmatrix} t_{d,j}^{on}(N) & if\ j \neq j_{max}^{on} \\ t_{d,j}^{on}(N) + t_d^{on} & if\ j = j_{max}^{on} \end{Bmatrix}$$

Turn-off condition:

$$t_{d,j}^{off}(N+1) = \begin{Bmatrix} t_{d,j}^{off}(N) + t_d^{off} & if\ j \neq j_{max}^{off} \\ t_{d,j}^{off}(N) & if\ j = j_{max}^{off} \end{Bmatrix}$$

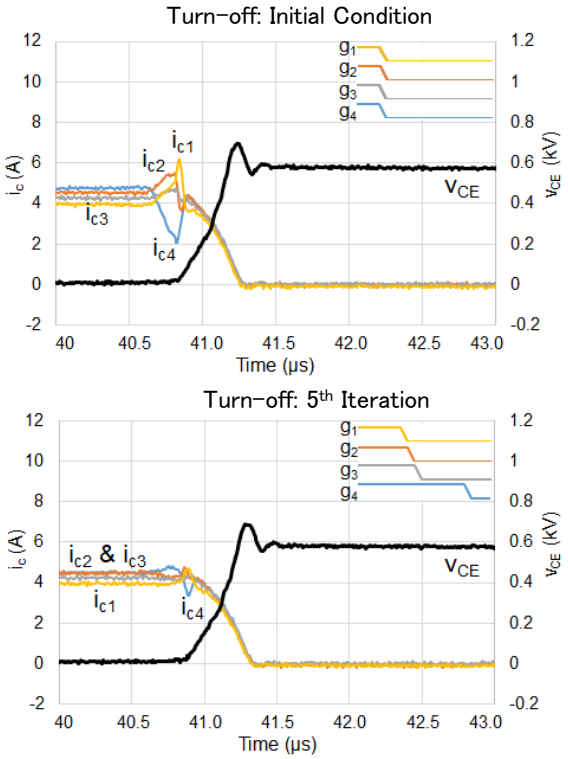

Fig.4b Measured IGBT currents for four parallel connected IGBTs during turn-off.

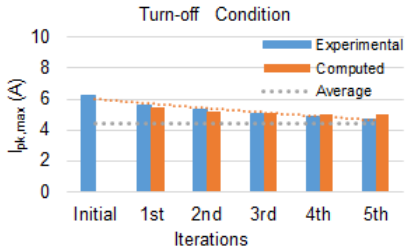

Fig.5b Maximum peak current minimization trend during turn-off condition.

t_d^{on}, t_d^{off} are unit delay time for turn-on and turn-off respectively and $j_{max}^{on}, j_{max}^{off}$ defined for the conditions as:

$$I_{pk,max}^{on} = I_{pk,j}^{on}, I_{pk,max}^{off} = I_{pk,j}^{off}$$

The same or different unit delay time can be used independently for turn-on and turn-off delay control.

3.2.3 Evaluation of delay compensation:

The delay compensation among the gate signals is an easy and effective technique to minimize unbalancing for the paralleled system as well as widely applied for the series connected system too. Furthermore, the evaluation of delay compensation is required to analyze the trend of unbalance minimization.

The device rise-fall time and the switching delay time is the total effective delay time that can be used for gate delay compensation. Switching time and switching delay time is usually non-identical for turn-on turn-off therefore total effective delay time for compensation is unique for turn-on and turn-off.

The rise-time and switching delay combine together and termed as switching time for turn-on. Similarly, fall-time and switching delay combine together and termed as switching time for the turn-off. The rise and fall time provides the rate of change device current $(^{di}/_{dt})$ correspondingly for turn-on and turn-off.

The peak current minimization can be approximately evaluated using the following:

$$\Delta I_{pk,max} = e^{-m/n}$$

where m is the number of iterations and n is defined by

$$\mathrm{n} = \frac{I_{pk,initial}}{t_d * (^{di}/_{dt})(N_p - 1)}$$

where N_p is a number of parallel connected IGBT.

4. Experimental test and validation

4.1. Experimental system

The experimental system of four parallel connected discrete IGBTs represented as the schematic diagram shown in Fig.3, is used to validate and test the effectiveness of gate delay control for active current balancing and peak current minimization. The gate delay control including peak detection is digitally implemented in Zedboard evaluation and development FPGA board having a fundamental clock frequency of 100MHz. This allows the minimum possible unit delay of 10ns that can be used for delay lines.

The control implementation uses only 5% of the overall computational capacity of FPGA that features the simplicity of the algorithm. Moreover, the real-time implementation of developed control uses total 5 clocks of FPGA to generate controlled gate signal. To avoid the possibility of jitter in enable signals, clock signal of 50MHz were used that cost 100ns corresponding to 5 clocks to complete digital computation for generation of next sequence of gate signals.

4.2. Results and Validation

The paralleled IGBT system was possessing inherent unbalancing during turn-on, however, there were no unbalancing during turn-off. The unbalancing was manually incorporated in the system by using an unequal gate resistance. IGBT2 to IGBT4 were having equal gate resistances of 10Ω and IGBT1 was having unequal gate resistance of 11Ω. The unequal resistance introduced significant current peak unbalancing during turn-off.

At the initial condition, current unbalancing occurred in the system during turn-on and turn-off as demonstrated in Fig4a and Fig4b respectively. The unbalancing enabled the gate delay control through peak detection of individual IGBT current. Furthermore, automatic delay compensation of gate signals enabled the active current balancing to suppress maximum IGBT current overshoot unbalancing as shown in Fig.4a and Fig.4b for turn-on and turn-off respectively. Moreover, $I_{pk,max}$ minimization corresponding to a number of iterations, is demonstrated in Fig.5a and Fig.5b for turn-on and turn-off conditions respectively. The maximum peak current overshoot minimization almost followed an exponential trend.

5. Conclusion

This paper presents, the peak minimization based active current balancing that is capable of independent delay control during turn-on and turn-off condition. The effectiveness of gate delay compensation to suppress the maximum current peak overshoot and achieve active current balancing is tested and validated experimentally for four discrete parallel connected IGBT under unbalanced conditions.

The current peak minimization is almost following an exponential trend corresponding to gate delay control iterations. Consequently, the dynamic current sharing has also improved among the paralleled devices.

Acknowledgments

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