Investigation of Relation between Switch Timing Difference and Common-mode Voltage on Cable

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Abstract – **Recent equipment uses many inverters from the viewpoint of energy saving. The inverter circuits have a potential of disturbance source because the high voltage and high speed switching devices are used in the circuits. In this paper, we investigated the relationship between the switch timing difference of inverter circuit and the common-mode voltage on the cable. First, we investigated the mechanism generating the common mode voltage by using the inverter system which was used for driving a three phase motor. A simple equivalent circuit of the system was created. And then, the mechanism was evaluated by the circuit simulation. The results showed that the switch timing difference caused the common-mode voltage. Next, the drive circuit was constructed by using CPLD, and the common-mode voltage was measured by capacitive voltage probe (CVP). The results showed that the common-mode voltage increased by the increase of the switch timing difference and the influence mainly appeared below 1 MHz.**

Keyword: Inverter, Common-mode voltage, Switch timing

I. INTRODUCTION

The number of equipment using inverters increases according to the development of energy saving technology. The inverter causes the disturbances emission because this uses a high voltage and a high speed switching circuit. Therefore, the radiation mechanism and the method of countermeasure have been studied [1] – [4].

The drive circuit of three phase motor uses an inverter circuit. Therefore, the radiation mechanism of disturbances was studied and the paper [2] pointed out the common-mode current on the motor drive cable is the emission source above 30 MHz. However, the reason why the emission more than 100 MHz appears on the common-mode current has not been clear.

In this paper, we examined the relationship between the common-mode voltage and the switching timing difference. First, the principle of generating common-mode voltage by the switch timing difference is discussed by the drive system of three-phase motor. Next, the effect of the switch timing for the common-mode voltage is simulated by simple equivalent circuit. Finally, the relation between the common-mode voltage and the switch timing difference is evaluated by the drive circuit using a CPLD.

II. DISTURBANCE BY SWITCHING TIMING DIFFERENCE

Figure 1 shows the example of the drive system for three phase motor. The system is constructed with a drive circuit, a drive cable, and a motor. The drive circuit is constructed with six field effect transistors (FETs) named U_U, V_U, W_U, U_B, V_B, and W_B. In these names, U, V, W present the phase name, and the subscripts of U and B indicate the upper derive device (FET) and the lower drive (FET) respectively.

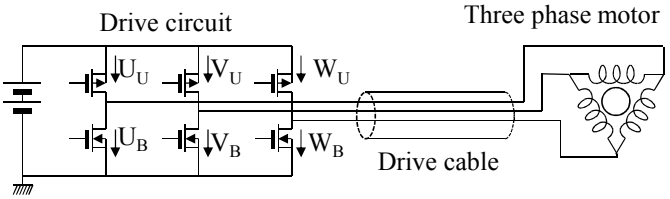


Fig. 1 Example of drive system for three phase motor

The example of control signal waveform of these FETs is shown in Fig. 2. In Fig. 2, N = 1 ~ 48000 represents the time step. The motor is rotated by switching the FET using this waveform. The rotation speed is controlled by changing the switching period which is presented by N= 48000 in this figure. The comb-shaped wave in Fig. 2 is used for the pulse width modulation (PWM), and the torque of motor is controlled by changing the duty ratio.

As shown in Fig. 2, the pair of FETs (U_U and U_B, V_U and V_B, W_U and W_B) does not turn on simultaneously in the case of three phase motor drive. This means that we need not pay attention to the operation of the pair of FETs (ex. U_U and U_B) for preventing the damage of FET.

Figure 3 shows the simple model for investigating the influence of the switch timing. In this model, FETs is presented by switches, resistances of r_0 present the resistance of drive cable, and r_i(i=1~3) present a three phase motor. Although the equivalent circuits of the drive cable and the motor are presented by impedances at the actual condition, the impedances are replaced by resistances because of simplification.

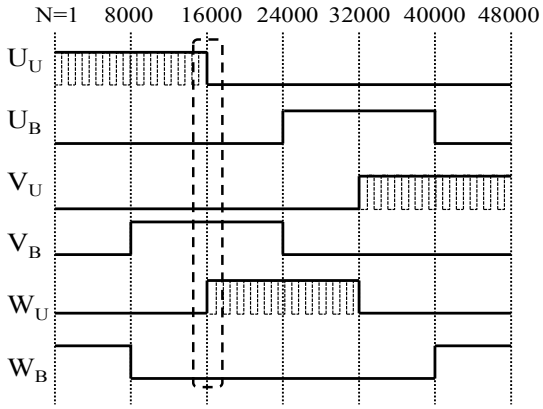
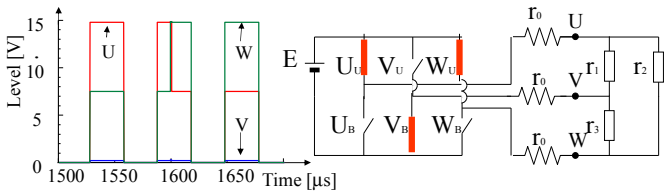


Fig. 2 Example of drive signal waveform

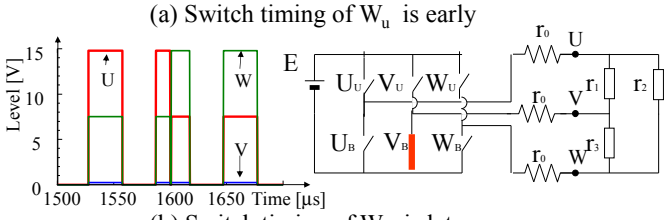
The left side graphs in Fig. 3 present the waveform when N is from 15000 to 17000 in Fig. 2. On the calculation, the voltage source level (E) of 15 V, the time step of 0.1 μs, r_0 of 1 Ω, and r_i of 100 Ω were selected. The resistance of switch when this was "ON" was 0.1 Ω and the resistance of switch when this was "OFF" was 1 MΩ. For the PWM, the waveform, whose period was 60 μs and duty ratio was 50%, was used.

When the switch of W_U turn on at N=15990 (1 μs early), both U_U and W_U are "ON" as shown in Fig. 3(a). And then, the voltage level at the point W in Fig. 3(a) changes from 7.5 V to 15V as shown in Fig. 3(a). The level at the point of U is 15V because the switch of U_U is "ON", and the level at the point of V is 0V because the switch of V_B is "ON".

When the switch of W_U turn on at N=16010 (1 μs later), the switches of U_U, V_U, and W_U are "OFF" as shown in Fig. 3(b). And then, the voltage level at the point W in Fig. 3(b) changes from 7.5V to 0V. The voltage levels at the points of U and V are 0V because the switches of U_U and V_U are "OFF" and the switch of V_B is "ON".



(a) Switch timing of W_u is early



(b) Switch timing of W_u is later

Fig.3 Simple model for investigating influence of switch timing

The common-mode voltage was calculated for investigating the influence of the switch timing. In this paper, the common-mode voltage was defined by equation (1).

$$V_C = \frac{V_U + V_V + V_W}{3} \qquad (1)$$

where, V_U, V_V, and V_W are voltage between each point (U, V, and W) and ground

Calculation results from N=15000 to N=17000 are shown in Fig. 4. The influence of the switch timing appears at N=16000. However, the larger common-mode voltage appears caused by the PWM operation.

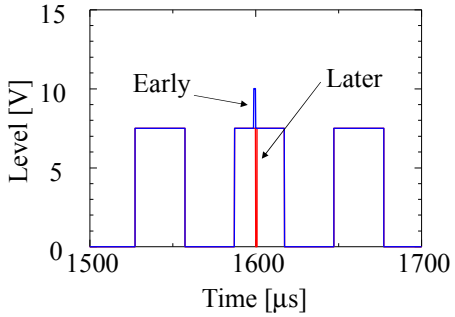


Fig. 4 Common-mode voltage caused by switch timing

III. DRIVE WAVEFORM FOR INVESTIGATION

Figure 4 shows that the disturbance appears caused by the switch timing. However, the level is lower than the level by PWM operation. Therefore, the drive waveform shown in Fig. 5 was employed to investigate the influence of switch timing.

The drive signal waveform in Fig. 5 applies PWM to both upper FET and lower FET. The drive system is balanced by applying to both side, and the common-mode voltage caused by the PWM is reduced.

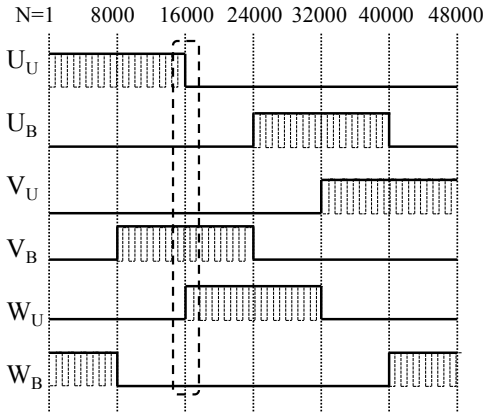


Fig. 5 Drive signal waveform used for investigation

The calculation results of the common-mode voltage from N= 15000 to N=17000 in Fig. 5 are shown in Fig. 6. The model and the conditions in Fig. 3 were used for the investigation. The duty ratio of the PWM is 50% at original position and the timing of W_U is changed to N=15990 (early) and to N=16010 (later). In addition, the duty ratio of U_U and W_U were changed to 48% (early) and to 52% (later).

This shows that the common-mode voltage caused by the PWM is reduced and the voltage by the timing difference only

appears. This means that the common-mode waveform is convenient to investigate the influence of the FET switch timing difference.

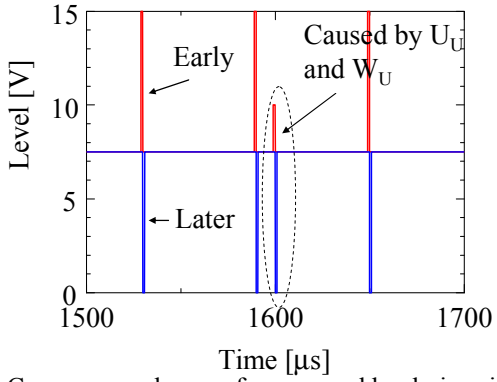


Fig. 6 Common-mode waveform caused by derive signal in Fig. 5.

IV. Evaluation of Common-Mode Voltage

The influence to the common-mode voltage by the switch timing difference was investigated by a simple experimental system. The investigation result is described in this section.

A. Configuration of the drive circuit

Figure 7 shows the external view of the drive circuit for the investigation. The CPLD whose clock frequency was 64 MHz was used for the signal oscillator. The switch timing of the FET was controlled by changing the VHDL program of CPLD. The Si4532 (Vishay Siliconix) which was built N-channel and P-channel MOS-FET into a single package was used as the drive FET. The BS870 (Diodes) was used to drive the upper side FET. DC link voltage of the inverter was 15V

The drive signal period generated by CPLD was 24 ms, PWM wave period was 60 μs and the duty ratio of PWM was 50% for U_B, U_U, V_U, W_B, and W_U. Moreover, the duty ratio of V_B was changed from 50% to 48% by VHDL program.

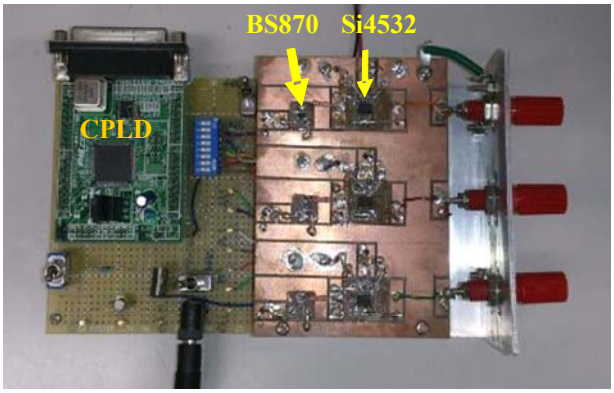


Fig.7 External view of drive circuit used for investigation

Figure 8 shows the example of measured drive waveform. The waveform whose period was 24 ms was observed. This means the drive circuit in Fig. 7 operates according to the design specification and the drive circuit can be used for the investigation.

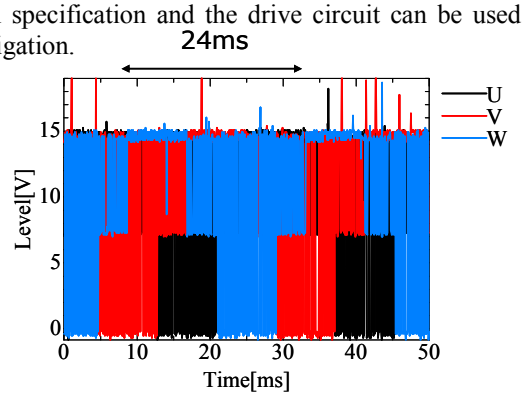


Fig. 8 Example of drive waveform by drive circuit

Experimental set-up for measuring common-mode voltage is shown in Fig. 9. The drive circuit in Fig.7, the drive cable, and the load were placed on the metallic ground plane. Vinyl insulated Vinyl sheathed Flat-type cable (VVF cable) whose length was 1 m was used as the drive cable. The diameter of the conductor was 1.6 mm. The three phase motor which was the load of the cable was presented by the impedance. However, the impedance was indicated by the resistor of 100Ω for simplification of the model.

The common-mode voltage was measured by capacitive voltage probe (CVP) [5] and a spectrum analyzer. The CVP whose operating frequency range was from 100 kHz to 100 MHz was used for the experiment. The CVP was placed 40cm away from drive circuit. The height of cable was determined from the height of CVP, and the height is set to 10 cm. The high pass filter, whose cutoff frequency was 110 kHz, was inserted at the input port of the spectrum analyzer to prevent the large drive signal.

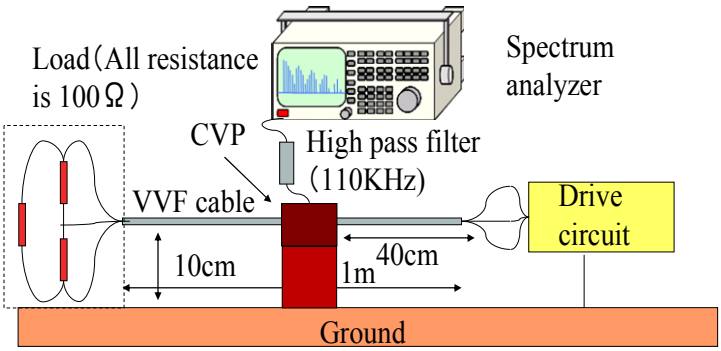


Fig. 9 Experimental set-up for measuring common-mode voltage

Figure 10 shows the measurement results. In this figure, the duty ratio of V_B was changed from 50% to 48%, and the spectrum was measured. The RBW and VBW of spectrum analyzer were 9 kHz and 100 kHz respectively.

This shows the spectrum decrease in proportion to the frequency. The spectrum does not changed by changing the duty ratio of V_B in frequency range from 10 MHz to 100 MHz. However, the spectrum when the duty ratio is 48% is larger

than that of the duty ratio of 50% in frequency range below 10MHz.

The average value in the specified frequency band was evaluated to confirm the tendency shown in Fig. 10. The result is shown in Fig. 11. In this figure, the vertical axis shows the average value defined by the equation (2).

$$A = \frac{1}{N}\sum_{i=1}^{N} V_{Ci} \qquad (2)$$

In this equation, N is the number of the spectrum in the specified frequency band, and V_{ci} is voltage level of each spectrum. Three bands which were 0.15~1MHz, 1~10MHz, and 10~100 MHz were selected for the investigation. The vertical axis is the level normalized by the level at the duty ratio of 50%. This shows that the average value increases under inverse proportion to the duty ratio in frequency range from 0.15 MHz to 1 MHz. On the other hand, the average value does not increase in frequency range from 10 MHz to 100 MHz when the duty ratio is less than 49%. This means that the influence of the switch timing difference mainly appears below 1 MHz.

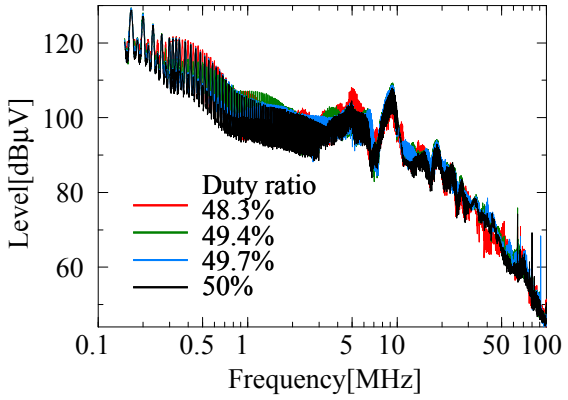


Fig. 10 Common-mode voltage spectrum appearing on drive cable

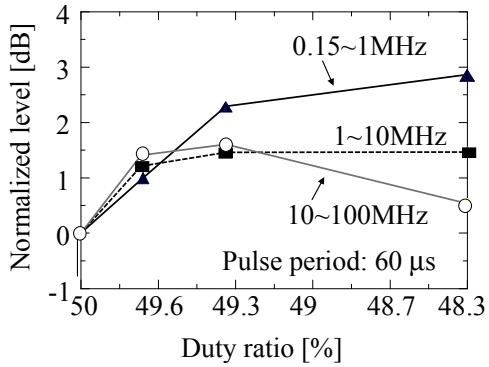


Fig. 11 Relation between average voltage and delay time

VI.CONCLUSION

The influence of switch timing difference in the inverter circuit which was used to drive three phase motor was investigated. The motor drive system is modeled a simple circuit to study the disturbance generation mechanism. The results showed that the switch timing difference generated the common-mode voltage which was a disturbance source. The drive signal, which had PWM at both upper side and low side, was used to reduce the common-mode voltage in the investigation.

The drive circuit was constructed with CPLD and FET to investigate the relations between the common-mode voltage and the switch timing difference. The common-mode voltage was measured by using capacitive voltage probe (CVP) and a spectrum analyzer. The results showed that the influence of the switch timing difference mainly appears in the frequency below 1MHz. This result is used to reduce the disturbance caused by the inverter.

Future work is the investigation of the switch timing difference by PWM waveform and the study of disturbance generation by other mechanism.

REFERENCES

[1] J. Knockaert, J. Peuteman, J. Catrysse, R. Belmans, "Simulation of stair stepping on inverter-fed induction motors," emc euraope 2006 barcelona, pp.230-235, Sep. 2006

[2] Ran Wang, Nobuo Kuwabara, Kiyoshi Masui, and Hideya Sato, "Investigation on mechanism of radiated emissions from fan unit model," Proceedings of the 18th international Zurich symposium on electromagnetic compatibility, Munich, pp. 437-440, Sep. 2007.

[3] Yasuhiro Shiraki, Yuichi Sasaki, and Noto Ok, "Conductive noise analysis for automobile inverters by equivalent circuit, " IEICE Technical Report, EMCJ2012-126, March 2013 (in Japanese)

[4] Keong Kam, David Pommerenke, Ankit Bhargava "Analysis and Mitigation Techniques for Broadband EMI from Synchronous Buck Converter", 2012 IEEE Electromagnetic Compatibility Magazine − Volume 1 − Quarter 3 pp.28-38

[5] Hideaki Takahashi, Nobuo Kuwabara, Fujio Amemiya, and Mitsuo Hattoroi, "Method of measuring voltage without cable correction by loading capacitance changeable CVP," Proceedings of the 18th international Zurich symposium on electromagnetic compatibility, Munich, pp. 482-484, Sep. 2007