Physical Design Guides for Substrate Noise Reduction in CMOS Digital Circuits

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***Abstract*—Substrate noise injection in large-scale CMOS logic integrated circuits is quantitatively evaluated by 100-μV 100-ps resolution substrate noise measurements of controlled substrate noises by a transition-controllable noise source and practical substrate noises under CMOS logic operations. The noise injection is dominated by leaks of supply/return bounce into the substrate, and the noise intensity is determined by logic transition activity, according to experimental observations. A time-series divided parasitic capacitance model is derived as an efficient estimator of the supply current for simulating the substrate noise injection and can reproduce the measured substrate noise waveforms. The efficacy of physical noise reduction techniques at the layout and circuit levels is quantified and limitations are discussed in conjunction with the noise injection mechanisms. The reduced supply bounce CMOS circuit is proposed as a universal noise reduction technique, and more than 90% noise reduction to conventional CMOS is demonstrated.**

***Index Terms*—Mixed analog–digital integrated circuits, power supply current modeling, reduced supply bounce CMOS circuit, signal integrity, substrate coupling, substrate measurements, substrate noise reduction.**

I. Introduction

THE application areas of analog–digital mixed-signal CMOS designs have greatly expanded. Read channel circuits for storage devices, interface electronics for fast networking media, single-chip wireless transceivers with baseband signal processors, and CMOS functional imagers for personal mobile terminals are typical examples. Sub-quarter-micron technology is currently available for mass production of devices for these applications, where dies integrate million-gate digital macro-cores with wide-dynamic-range and/or high-frequency functional analog circuits.

Crosstalk from digital circuits is mainly leaks of digital switching noise into analog components, mostly via substrates and thus named substrate noise. Such noise degrades analog signal integrity in mixed-signal IC designs. The noise interferes with analog circuit operations and then causes unallowable tones or distortions within a signal bandwidth of the analog signal processing [1]–[4]. In addition, even in high-end digital macro-cores, the noise can affect dynamic behaviors of logic circuits. Change in threshold voltage due to the substrate voltage fluctuation results in variations of subthreshold leakage and of subthreshold slopes among MOSFETs, which leads to erroneous toggles and timing faults. This also gives rise to serious signal integrity issues. On the other hand, in emerging socket-based design styles, much effort has to be made to maintain circuit performance specifications under various combinations of digital and analog reusable IP cores located on the same noisy substrate while also meeting the required short turnaround. These noise issues have been widely recognized as critical problems to solve, since the implementation of mixed-signal systems-on-a-chip (MS-SoC) VLSI circuits have become a practical solution to those industrial applications.

There are some remedies at a material level. Use of silicon-on-insulator (SOI) or triple-well technology can isolate analog partitions from their digital counterparts by surrounding oxides. However, unavoidable frequency dependence of the electrical isolation due to ac coupling at device-to-substrate borders [5], [6] and the increase in manufacturing costs due to extra process steps are discouraging. Lowering parasitic impedance between the substrate and a system ground at the assembly stage is another approach. This includes, for instance, multiple wire bondings to reduce parasitic inductance, and eutectic alloying to obtain low resistivity ohmic contacts at the interface of the substrate backside and a metallic plate in the package cavity. Because of the difficulties in quantitative estimation of effectiveness, these are considered supplementary treatments.

Successful MS-SoC IC designs necessitate substrate noise management at algorithm, circuit, and layout levels. Full-chip substrate noise verification is one of the key technologies for this task. It helps designers control the noise influence on system performance and eases design optimization for minimizing noise interference. For practical verification, it is necessary to have efficient simplification methods for modeling the substrate crosstalk process which methods include noise current injection in large-scale logic circuits, propagation in a silicon substrate and interactions with surrounding parasitic memory/memoryless elements, and the noise sensitivity in victim circuits. Many excellent developments have been reported [7]–[13], and intensive studies are continuing.

Another technical direction for achieving the above task lies in the development of noise reduction techniques. Guardband placements between logic circuits and sensitive analog circuits have conventionally been adopted. Optimized decoupling circuits can effectively dump low-frequency supply/return bounce

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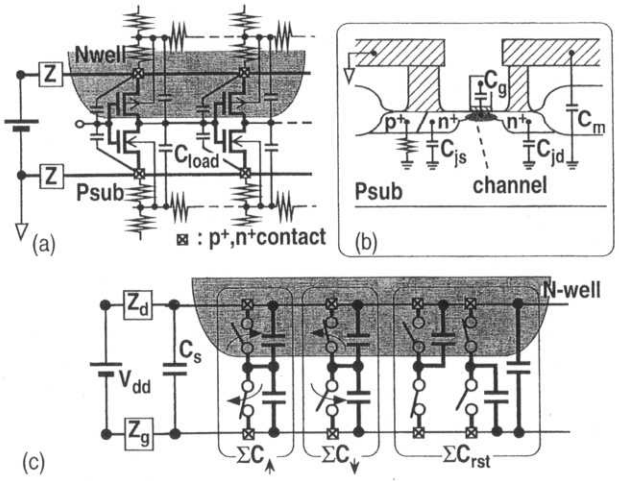

Fig. 1. (a) Simplified schematic of conventional CMOS inverters. (b) Cross section of an n-type MOSFET in the inverter. (c) Charge transfer in large-scale logic operations.

[14]–[16]. In addition, active guardband filtering technique has been reported [17].

It is essential to understand the basic behaviors of the noise itself and the principles of the noise reduction techniques in order to improve substrate noise management. This paper focuses on the substrate noise injection processes in CMOS digital circuits and design techniques for effective noise reduction. Section II gives an overview of the major noise injection mechanisms, and Section III discusses basic characteristics of the substrate noise through detailed analyses of the high-resolution quantitative substrate noise measurements of controlled substrate noises by a transition-controllable noise source. The factors decisively governing the noise intensity are defined. In Section IV, the experimental analyses are expanded to practical CMOS logic circuits, and an advanced noise source simulation model is derived from the obtained knowledge. Subsequently, in Section V, we propose a universal substrate noise reduction principle that is fully compatible with conventional CMOS logic designs and demonstrate a reduced supply bounce (RSB) CMOS circuit based on this principle. In addition, the effectiveness of the proposed and conventional noise reduction techniques is quantitatively evaluated in order to establish practical physical design guides for substrate noise reduction. Section VI provides our conclusions.

II. Substrate Noise Injection in CMOS Logic Circuits

Most CMOS logic elements can be reduced or decomposed into CMOS inverters. Fig. 1(a) shows a schematic diagram of the CMOS inverter in a typical p-type bulk substrate with n-type single-well technology. When the logic state of the inverter toggles, charging current flows to the load capacitance ($C_{\rm load}$) and noise current is injected into the substrate. Three major noise currents should be considered: capacitively coupled (CC) current through $C_{\rm load}$, impact ionization (II) current at the drain end of a MOSFET, and current due to voltage bounce on the supply/return rails.

Parasitic capacitances of a MOSFET at the source/drain diffusions (C_{js}, C_{jd}) and at the gate electrode (C_g), and that of the lower level wire capacitance (C_m) against the substrate are defined in a cross section of an n-type MOSFET composing the inverter, as depicted in Fig. 1(b). The load capacitance is composed of C_{jd} at the output and a total sum of C_m and C_g belonging to the inputs of subsequent logic elements. Since the capacitance per unit area and periphery for C_g is a few times larger than C_{jd} in advanced MOS devices with an ultrathin gate-oxide film and the average fan-out value over logic gates in a digital macro-core is generally more than two, $C_{\rm load}$ is dominated by C_g. It can be approximately estimated that C_g/C_{jd} of 1 μm^2 is 4, and the areal ratio of the gate to drain electrodes is $1/2$ in standard logic cells in a typical 0.35-μm CMOS technology. Because the use of the lowest level interconnect wires is limited to intergate short nets and the upper-level interconnect wires used for long nets are routed over the MOSFETs, the wire capacitance against the substrate is negligible in a dense logic cell array. Therefore, the greater part of CC currents flows directly into the source electrode through C_g, which is the capacitance between the gate electrode to a sheet electron channel formed beneath the gate electrode in an on-state MOSFET, and then drains off to a system ground via the metallic wires. The rest of the current is injected into the substrate and mostly flows toward the nearest substrate contacts, which are often adjacent to the source electrode, as shown in Fig. 1(b). Finally, a small portion of the injected current spreads within the substrate.

The origin of the impact ionized current is a creation of electron/hole pairs by a strong electric field along the channel of a MOSFET. The pairs are split by the field, and then hole current flows in the substrate toward the nearest substrate contacts while the flux of the electrons penetrates into the gate oxide. Although II current grows much larger for the smaller gate-length MOSFETs beyond the subquarter-micron technology, it is still minor compared to CC current for the single inverter circuit operating at several tens of megahertz or more [18].

From this microscopic view of the noise current injection processes in the inverter operation, we can conclude that the direct contribution of CC and II currents to the substrate noise is small, as long as the victim circuits are separated from the noise source at a certain distance. Note that this does not apply to those circuits with very densely packed aggressor–victim pairs such as in oscillators, image sensor pixels, and so forth. On the other hand, the leakage of the voltage bounce on the supply/return rails into the substrate dominates the substrate noise injection in large-scale digital blocks. A macroscopic view of this process is provided as follows.

The collectives of $C_{\rm load}$ in a large-scale logic block can be dynamically classified into three groups, as shown in Fig. 1(c): the groups of the capacitances belonging to the logic elements that switch in rise ($C_{\uparrow}$), that switch in fall ($C_{\downarrow}$), and that remain in current states ($C_{\rm rst}$). The impedances of Z_d and Z_g are parasitic to the supply and return path, respectively, between the die and an external power source ($V_{\rm dd}$). C_s stands for a static capacitance including decoupling capacitors and n-type well junction capacitances.

The fast switching operations in CMOS logic circuits are realized by charge redistribution among the spatially distributed parasitic capacitances within the block, where C_s and $C_{\rm rst}$ serve as local charge reservoirs. Because currents made by this

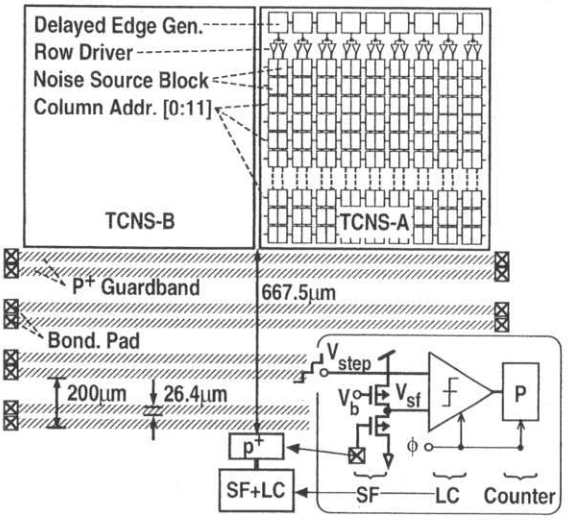

Fig. 2. Overview of substrate noise evaluation chip. Linear substrate noise detector (SF+LC) is shown in the inset.

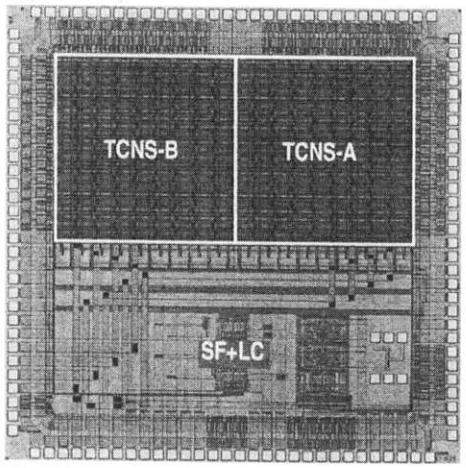

Fig. 3. Microphotograph of substrate noise evaluation chip.

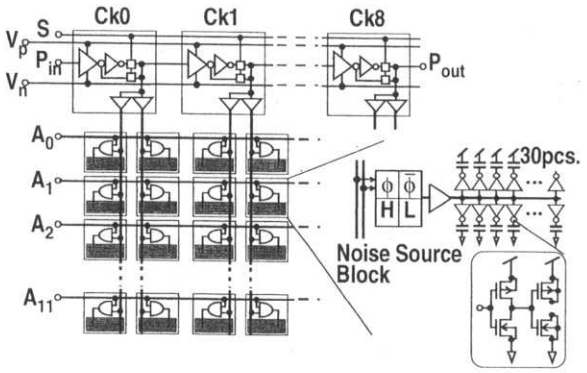

Fig. 4. Transition-controllable noise source circuit.

process are again immediately absorbed into these capacitances, their contribution to substrate noise is minor. This absorption is mostly through the metallic supply/return wires, channels of on-state MOSFETs, and the gate-to-channel capacitances of MOSFETs involved in $C_{\rm load}$. On the other hand, the external power source supplies consumed charge in the redistribution process and completes the switching operations. The resultant supply current interacts with Z_d/Z_g and shows changes with a time constant to the degree of $(Z_d + Z_g) \cdot C_{\rm par}$, where $C_{\rm par}$ denotes the entire parasitic capacitance in the digital block. Since the substrate is tightly coupled to the return path by distributed surface substrate contacts, the voltage bounce arising from this process, especially on the return path, appears as substrate noise.

Previous measurement results closely match this view and are discussed in [19] with more detailed analyses of the substrate noise waveforms.

III. Basic Characteristics of Substrate Noise

A. Test Chip Design

Further investigations of the substrate noise injection process were performed in order to define the factors determining the noise intensity [20]. The substrate noise evaluation chip, shown in Fig. 2, was developed in a 0.6-μm CMOS p-type bulk substrate with a single n-type well, triple-layer metal, and double-layer poly-Si technology. All of the circuits were designed with a supply voltage of 3.3 V. A chip microphotograph is shown in Fig. 3. The chip includes two transition-controllable noise sources (TCNS-A, TCNS-B), a linear substrate noise detector (SF+LC), and four pairs of p^+ guardbands (GBs) located at equal spacing between the noise source and the detector.

Fig. 4 shows a redesigned version of the TCNS [19]. The circuit has a nine-stage delayed-edge generator (Ck[0:8]) and an array of noise source blocks selectively activated by those edges with selection bits (A[0:11]). The array ($N_{\rm array} = 9 \times 12$) is doubled and thus two noise source blocks are located at every intersection of Ck[0:8] and A[0:11]. We hereinafter call these arrays the left and right arrays. The noise source block has 30 noise injectors consisting of a CMOS inverter with load capacitors formed by the gate-to-channel capacitances of n- and p-type MOSFETs and a programmable driver stimulating the noise injectors. The driver can be programmed for each array to generate output transitions in-phase or out-of-phase to the incoming edge and also to be stable at a logical high or low state. Tapered multiple drivers are provided between the edge generator and the programmable driver and optimized to a noise injector switching time of less than 200 ps for both rise and fall transitions. The TCNS can generate substrate noises under specified conditions to control the interstage delay time, the interstage edge direction, and the number of active noise source blocks per edge.

The difference between TCNS-A and TCNS-B lies in the power supply ($V_{\rm dd}$) routings, as depicted in the simplified diagram of Fig. 5(a) and (b). While each of the noise source block arrays has an independent $V_{\rm dd}$ system in TCNS-A, both arrays share a single $V_{\rm dd}$ system in TCNS-B. Every $V_{\rm dd}$ path for the TCNS is connected to an external power source beyond decoupling capacitors proximate to the chip on the device under test (DUT)—printed circuit board (PCB). On the other hand, the return (GND) paths are always common to the substrate nodes in a conventional single n-type well CMOS digital design. Here, Z stands for impedance parasitic to the $V_{\rm dd}$ or the GND paths, including bonding wires, package leads, and PCB wirings.

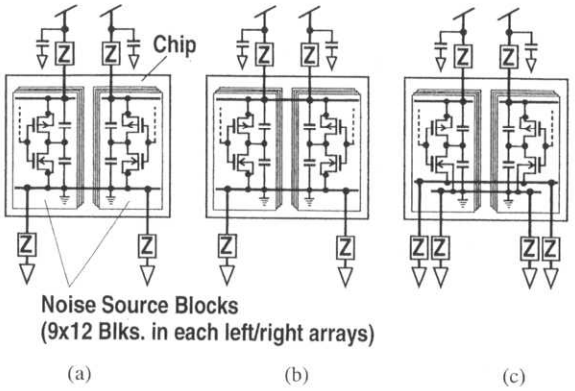

Fig. 5. Supply/return routing diagrams. (a) TCNS-A. (b) TCNS-B. (c) Kelvin grounding version of TCNS-A.

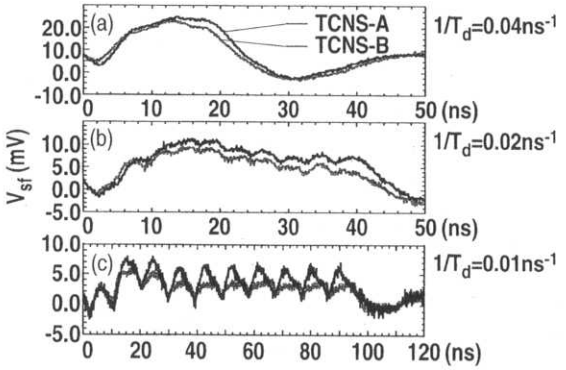

Fig. 6. Measured substrate noise waveforms by TCNS-A and TCNS-B for $N_{\rm blk} = 12$. Total delay time T_d is a parameter.

Quantitative substrate noise evaluation in a 100-ps 100-μV resolution is realized by using the linear substrate noise detector (SF+LC) shown in Fig. 2. The substrate voltage picked up by a p^+ contact probe is sensed by a p-channel source follower (SF) and then the shifted voltage ($V_{\rm sf}$) is sampled and digitized by an on-chip latch comparator (LC). The decision timing of the comparator is shifted relatively to the stimulus pulse or vectors input to the noise generator, and repetitive digitization gives a record of the substrate noise waveform. The detector gain calibrated by external reference sine waves was -3.7 dB, thus multiplication of $V_{\rm sf}$ by 1.5 roughly gives absolute values in the following measurement results. More detailed descriptions of the measurement principles, the measurement systems, and the detector circuits are provided in [19].

B. Quantitative Evaluation of Substrate Noise Injection

Typical substrate noise waveforms obtained for TCNS-A and TCNS-B are shown in Fig. 6, where every delayed edge is in a rise transition and activates twelve noise source blocks in the right array. Total delay time T_d in the edge generator, which is evaluated as the time difference between the stimulus edge input to $P_{\rm in}$ and the delayed edge appearing from $P_{\rm out}$, is parameterized. All of the noise source inverters in the left array are fixed in the low state, and GBs are floated. Horizontal and vertical axes show the elapsed time after the stimulus edge is input to $P_{\rm in}$, and $V_{\rm sf}$ digitized by the latch comparator, respectively. Offset voltage of the source follower is subtracted in the vertical axis.

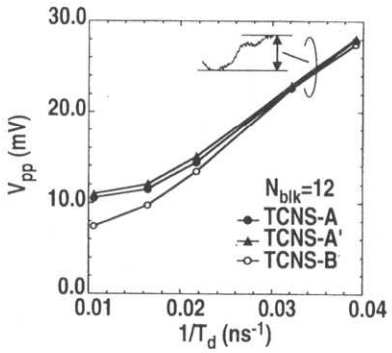

Fig. 7. Peak-to-peak substrate voltage $V_{\rm pp}$ versus inverse of T_d.

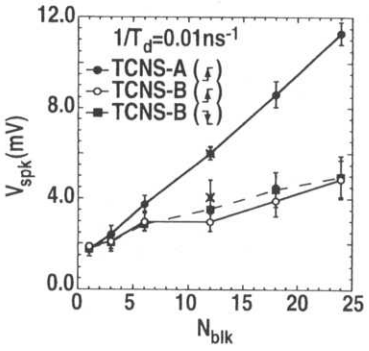

Fig. 8. Subpeak amplitude $V_{\rm spk}$ versus number of active noise source blocks $N_{\rm blk}$.

Low-frequency ringing dominates the waveform in Fig. 6(a), where T_d is minimized ($\sim$25 ns). As T_d increases, the ringing is suppressed and the subpeaks corresponding to the noise source transitions by the nine delayed edges become decomposed. Finally, the subpeaks dominate the waveform as in Fig. 6(c), where $T_d = 95$ ns.

Fig. 7 summarizes the dependence of the peak-to-peak substrate voltage $V_{\rm pp}$ on the interstage delay time. The $V_{\rm pp}$ increases roughly in proportion to $1/T_d$ in a smaller T_d domain where the ringing is dominant. The average supply current, which is also proportional to $1/T_d$, starts and stops flowing quickly and brings about large $L \cdot di/dt$ interaction in this region. On the other hand, $V_{\rm pp}$ becomes less dependent on $1/T_d$ in a larger T_d domain where the subpeak amplitude determines $V_{\rm pp}$. Obviously, the substrate noise amplitudes are smaller in TCNS-B than these in TCNS-A, and a distinct difference is observed in the domain where the subpeaks dominate, as Fig. 6(c) confirms. Fig. 7 also includes points for TCNS-A with the left matrix in an open circuit (without a $V_{\rm dd}$ connection) as TCNS-A$'$. The negligible difference between TCNS-A and TCNS-A$'$ indicates that Z is large enough to electrically isolate the parasitic capacitance in the left array from that in the right for the high-frequency supply currents relating to the observed substrate noises.

Fig. 8 summarizes the subpeak amplitude ($V_{\rm spk}$) versus the number of active noise source blocks ($N_{\rm blk}$) at $1/T_d = 0.01$ ns^{-1}. Each point shows a mean value and an error calculated from the peak-to-peak amplitudes of the nine subpeaks in the measured waveform. The cross marks at $N_{\rm blk} = 12$ are averages among five sample chips. The noise

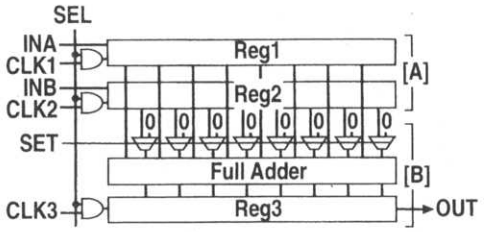

Fig. 9. Test circuit for substrate noise evaluation in practical CMOS logic operations. Sub-blocks [A] and [B] include two 8-bit shift registers and an 8-bit full adder with the output register, respectively.

amplitude is larger in TCNS-A than in TCNS-B whenever the same number of noise source blocks are operated. Moreover, the slope is approximately 3.4 times larger in TCNS-A, although $V_{\rm spk}$ for both TCNSs increases linearly with $N_{\rm blk}$.

The difference in the slope results from that in the activity. Average activities of $\mathrm{Act}(A)$ in TCNS-A and $\mathrm{Act}(B)$ in TCNS-B are as follows, where N_{blk_l} and N_{blk_r} are the number of blocks simultaneously activated in the left and in the right arrays. Here, $N_{\rm array}$ is the total number of noise source blocks belonging to each of the arrays.

$$\mathrm{Act}(A) = \frac{N_{\mathrm{blk}_l}}{N_{\rm array}} + \frac{N_{\mathrm{blk}_r}}{N_{\rm array}} \tag{1}$$

$$\mathrm{Act}(B) = \frac{N_{\mathrm{blk}_l} + N_{\mathrm{blk}_r}}{N_{\rm array} + N_{\rm array}}. \tag{2}$$

The TCNS-A can be considered to have two independent digital blocks with an average activity of $N_{\rm blk}/N_{\rm array}$ for each by virtue of the electrical separation of the high-frequency supply current of both blocks. On the other hand, TCNS-B can be treated as one large digital block, where a lump of numerous inactive noise injectors form a huge distributed-charge reservoir absorbing the supply current variation and effectively suppress the substrate noise. We have confirmed that measured waveforms rarely change if the $V_{\rm dd}$ connection on the left side is cut at just outside the chip in TCNS-B. These observations indicate that the activity in the logic block is the decisive factor of the noise intensity.

The results for the fall edges are also shown in Fig. 8. Consistency between the rise and fall edges results from the balanced n- and p-type MOSFET channel capacitances (Fig. 4) that dominate $C_{\rm par}$.

The effectiveness of the noise reduction techniques is another decisive factor and must be characterized quantitatively. This will be discussed in a later section.

IV. Substrate Noise in Practical CMOS Logic Circuits

A. Test Chip Design

To expand our explanation of the substrate noise injection process, which was deduced from the experimental process on a simplified noise source circuit, to practical CMOS logic circuits, a test circuit, shown in Fig. 9, was designed. The circuit has two logic sub-blocks: [A], two 8-bit shift registers (Reg1, Reg2), and [B], an 8-bit ripple-carry adder with an 8-bit shift register (Reg3). The adder has a selector signal for switching the operation modes of "Reg1 + Reg2" and "Reg1 + 0." While the sub-block [A] uses cells in a standard library, the sub-block [B] uses compound gates with stacked MOSFETs designed manually.

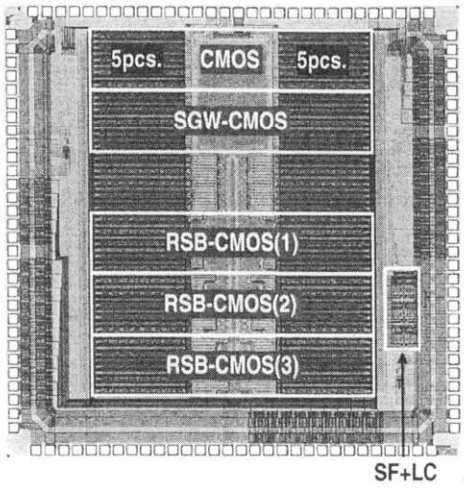

Fig. 10. Microphotograph of test chip.

A microphotograph of the test chip is shown in Fig. 10. The chip was fabricated in the same 0.6-μm CMOS production lots with the substrate noise evaluation chip. The chip includes five noise source modules, where ten pieces of the test circuit are arranged in a column structure for selective activation, and a SF+LC detector. One of the modules uses a conventional CMOS topology and the others are applied with reduced noise designs, which will be described in the next section.

B. Measurement Results

Quantitative substrate noise evaluations were carried out [21]. A test vector to the test circuit includes a simultaneous loading of a pair of serial 8-bit data into the register pair (Op1), the addition with the alternate input-mode switching (Op2), readout of the adder output in Reg3 with a comparison to the expected value for ensuring proper operations, and NOP (halted). The halted time is long enough to avoid overlap of the substrate voltage fluctuations repeated by the vectors. Measurement windows of 40 ns are placed within Op1 and Op2. A set of background substrate noises mainly by CMOS I/O drivers for every possible vector is measured in advance under the condition that none of the test circuits is operated while the generated test vector is input to the chip.

Measured substrate noises by the circuit in Op1 with a supply voltage of 3.3 V and clock frequency of 50 MHz are given in Fig. 11. The background noise is subtracted from the measurements and presented as $V_{\rm diff}$ in the vertical axis. The clock signal is also shown for the time reference. The similarity of curves where the number of test circuits operating $(N_{\rm blk})$ is parameterized with these taken with different input bit patterns validates the use of $V_{\rm diff}$ as the net substrate noise by the test circuit. Slightly larger noises appear for the loaded data patterns with the more frequent bit shifts, "01010101," "00110011," and "00000000," in order. This indicates activity dependence, but it seems that most of the activity arises from part of the circuit operation that are independent of the data, such as clocking.

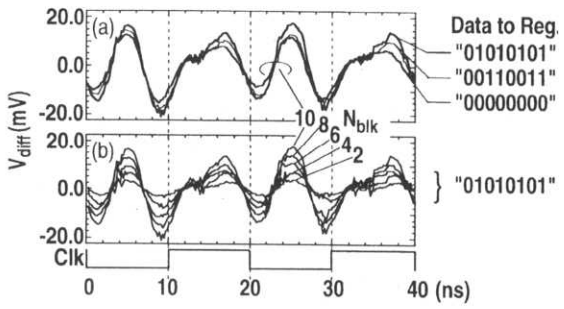

Fig. 11. Measured substrate noise waveforms by test circuit in conventional CMOS design, in Op1 at clock frequency of 50 MHz. (a) Bit pattern dependence. (b) Number of active test circuits is parameterized.

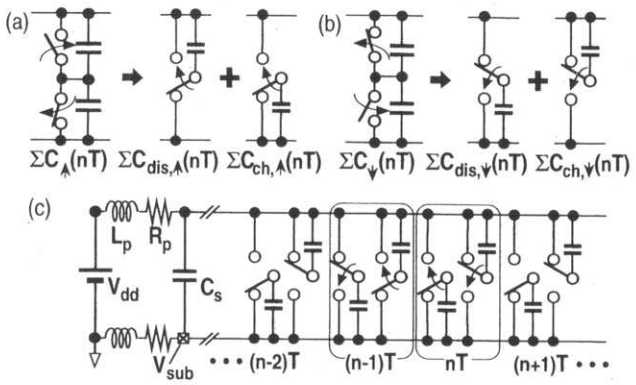

Fig. 12. Capacitances divided in nth interval. (a) Parasitic to logic elements switch in rise. (b) Parasitic to logic elements switch in fall. (c) Time-series divided parasitic capacitance model.

The linear increase in the noise amplitude with $N_{\rm blk}$ is as predicted from the observations in the transition-controllable noise source.

C. Analyses by an Equivalent Circuit Model of Substrate Noise Injection

We have demonstrated a simplified simulation model of the most dominant process in the substrate noise injection described in Section II for a transition-controllable noise source [19]. Further development of the model to expand it to practical CMOS logic operations is discussed in this section.

The groups of the capacitances parasitic to active logic elements [Fig. 1(c)] are again shown in Fig. 12(a) and (b) and are decomposed into the collectives of capacitances to be discharged ($C_{\rm dis}$) and to be charged ($C_{\rm ch}$). Here, the capacitances pulled up to $V_{\rm dd}$ and pulled down to GND correspond to the capacitances parasitic to p- and n-type MOSFETs, respectively. We introduce a time division to the continuous distribution of logic transitions for the purpose of modeling. Those groups accumulate the capacitances involved in the logic transitions occurring during the interval of $nT \sim nT + T$. Here, T and n stand for the period and the number of the interval, respectively. Charge transfer of $Q_\uparrow(nT) = \Sigma C_\uparrow(nT) \cdot V_{\rm dd}$ and $Q_\downarrow(nT) = \Sigma C_\downarrow(nT) \cdot V_{\rm dd}$, which is total required charge at every output node in a transition, takes place at every interval. The greater part of this process is immediately completed by the local charge redistribution between the active logic elements and the surrounding charge reservoirs made from $C_{\rm rst}(nT)$ and C_s. The entire digital block finally loses a charge of $Q_{\rm dis}(nT) = (\Sigma C_{{\rm dis},\uparrow}(nT) + \Sigma C_{{\rm dis},\downarrow}(nT)) \cdot V_{\rm dd}$ with an energy dissipation of $E_{\rm dis}(nT) = 1/2 \cdot (\Sigma C_{{\rm dis},\uparrow}(nT) + \Sigma C_{{\rm dis},\downarrow}(nT)) \cdot V_{\rm dd}^2$ by discharging currents that flow through shorted paths in those active logic elements with channel resistance of MOSFETs. On the other hand, a charge of $Q_{\rm ch}(nT) = (\Sigma C_{{\rm ch},\uparrow}(nT) + \Sigma C_{ch,\downarrow}(nT)) \cdot V_{\rm dd}$ is drawn from a power source and stored among these capacitances renewedly.

It is noteworthy that the role of the external power source is always to feed $Q_{\rm ch}(nT)$ into the digital block. The power source consumes the entire energy of $E_{\rm ch}(nT) = Q_{\rm ch}(nT) \cdot V_{\rm dd}$ in this process and is not involved in how the charging energy ($=E_{\rm ch}/2$) stored in the block is dissipated in later processes. A time-series divided parasitic capacitance model is derived from this fact, as shown in Fig. 12(c), that can be used as an efficient estimator of the supply current for simulating the substrate noise injection. It can also naturally estimate the activity dominating the noise intensity as described in Section III. Precomputed sets of $C_{{\rm ch},\uparrow}(nT)$ and $C_{{\rm ch},\downarrow}(nT)$ are connected to the supply/return rails for charging and then disconnected in the next interval of $(n+1)T$ by shorting. The charging process determines the supply-current waveform, accompanying the interaction with the parasitic impedance including L_p and R_p, while the discharging current contributes little to the return current. This process is repeated at every interval, and the supply current waveform is synthesized as a linear superposition of the currents due to the charge transfer of $Q_{\rm ch}$. Total energy dissipation in this model is equivalent to that in the original operation of the digital block.

Computation of $\{C_{{\rm ch},\uparrow}(nT), C_{{\rm ch},\downarrow}(nT)\}$ has to be carried out once for every possible input vector and can be done by integrating temporal toggle count distributions in every period of T, which distributions are acquired by full transistor-level circuit simulations or by gate-level HDL simulations. Note that the interval can be adaptively varied according to the activities in the logic block. The charge reservoir ($C_{\rm res}$) has to be estimated from the inactive elements and stable capacitors (C_s) and can be considered constant because the capacitance to be charged during the interval is very small. The parasitic impedances on the supply and return rails are assumed to be identical and represented as a series combination of an inductor (L_p) and a resistor (R_p).

The time-series divided parasitic capacitance models of the test circuit (Fig. 9) with $T = 250$ ps and also $T = 10$ ps are generated. Fig. 13 compares the substrate noise waveforms simulated with full transistor-level netlist [Fig. 13(a)] to that with the models [Fig. 13(b) and (c)] for the test vectors with input bit patterns of "00000000," "00110011," and "010101010" in the top, middle, and bottom figure, respectively, around the same rise clock edge. We chose $R_p = 1.2\ \Omega$ and removed L_p. Estimated $C_{\rm res}$ is 260 pF, including all of the noise source modules sharing primary supply/return paths and pads within the chip. Envelopes are very consistent among these waveforms for all of the vectors where the noise intensity obviously reflects the activity difference. Simulation time for ten clock periods (200 ns) was over 2500 s with the full transistor-level netlist that includes approximately 10K transistors. It was less than 10 s with both of the models by using HSPICE on a PA8500–440-MHz

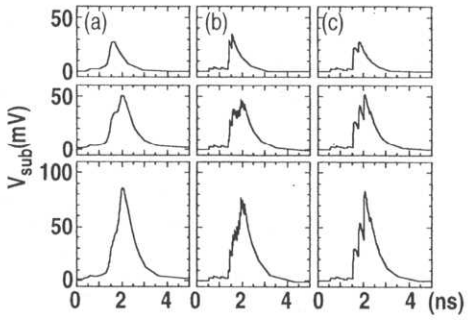

Fig. 13. Simulated noise waveforms. (a) Full transistor-level description. (b) Model of $T = 10$ ps. (c) Model of $T = 250$ ps. Test circuits work in Op1 with bit patterns of "00000000," "00110011," and "01010101" in the top, middle, and bottom figures, respectively. $R_p = 1.2\ \Omega$, without L_p.

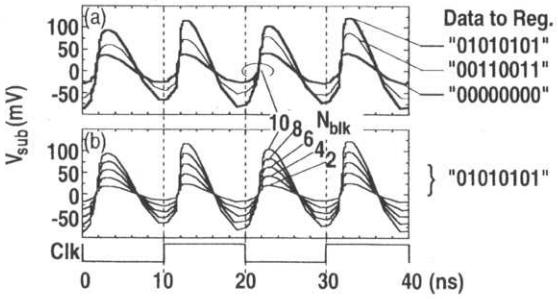

Fig. 14. Simulated substrate noise waveforms with the model of $T = 250$ ps in Op1 at clock frequency of 50 MHz. (a) Bit pattern dependence. (b) Number of active test circuits is parameterized.

CPU. Another set of simulated waveforms with the model of $T = 250$ ps, $R_p = 1.2\ \Omega$, and $L_p = 10.0$ nH is given in Fig. 14, which is comparable with the measured counterparts in Fig. 11. The value of L_p was adjusted to have the best similarity.

Simulations were effective in qualitatively reproducing the general features of the experimental results, and helped in understanding the substrate noise formation process. The model is efficient and accurate enough for estimating the substrate noise in the digital block under design. However, more sophisticated models of peripheral passive circuits for the interaction with the supply/return impedances and also well-established substrate mesh models for the attenuation of the noise intensity in the substrate propagation [2], [22]–[24] must be incorporated for quantitative improvements.

V. Noise Reduction Techniques and Effects

A. Layout-Level Noise Reduction

Guardbanding is the most popular noise-reduction technique for layout work. The effect of guardbands is quantitatively examined with the substrate noise evaluation chip described in Section III. The guardbands on that chip are filled with substrate contacts and run across the chip with dedicated bonding pads on both edges, which can be selectively shorted to a GND plane of the DUT board.

Fig. 15 summarizes the peak-to-peak noise amplitude $V_{\rm pp}$ and the subpeak amplitude $V_{\rm spk}$ versus the position of the pair of guardbands measured from the p^+ probe of SF, where the corresponding pair is connected to GND. The $V_{\rm pp}$ is dominated by ringing at $1/T_d = 0.04\ \text{ns}^{-1}$ and $1/T_d = 0.02\ \text{ns}^{-1}$, and the

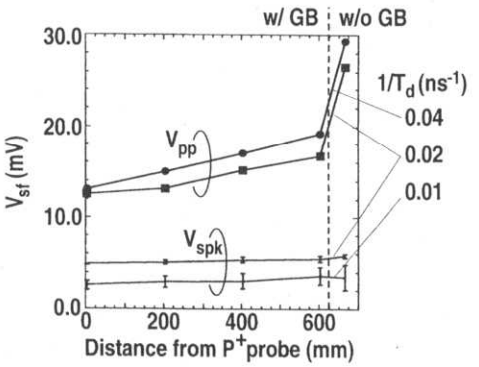

Fig. 15. Noise reduction effect versus guardband distance from detector. TCNS-A is used as noise source, $N_{\rm blk} = 12$ for $T_d^{-1} = 0.04\ \text{ns}^{-1}$ and $T_d^{-1} = 0.01\ \text{ns}^{-1}$, $N_{\rm blk} = 24$ for $T_d^{-1} = 0.02\ \text{ns}^{-1}$.

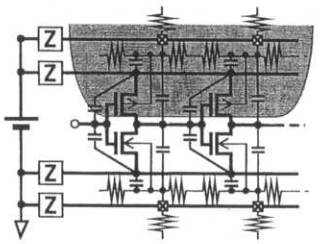

Fig. 16. Separate guard wiring CMOS circuit configuration.

$V_{\rm spk}$ dominates the waveform at $1/T_d = 0.01\ \text{ns}^{-1}$. In contrast to the strong reduction in $V_{\rm pp}$ in the ringing domain, $V_{\rm spk}$ changes little since the guardband effect deteriorates with larger noise frequencies due to an increase in Z parasitic to the path from the guardband to a system ground.

On the other hand, although the use of the nearest pair marks a 53% reduction in $V_{\rm pp}$, only a 3% increase is observed if the nearest half of the pair is grounded. Moreover, only a 6% improvement is obtained if all of the pairs are grounded in spite of the 300% area enlargement. Placing guardbands as close as possible to the sensitive circuit is most effective and a better way than widening.

As these observations indicate, the low-frequency ringing noise can be well reduced by the guardband during the propagation in the substrate; however, the high-frequency noise correlating to the logic activity has to be suppressed at the noise source during circuit operations.

B. Circuit-Level Noise Reduction

One way to reduce the noise at the source circuit is the isolation of the guard wirings for the substrate/well ties from the noisy $V_{\rm dd}$/GND wirings in the CMOS logic elements. This configuration is given in Fig. 16 and termed separated guard wiring (SGW) CMOS. The separation of the substrate ties and return rails is often called Kelvin grounding. Some of the industrial ASIC cell libraries for high-performance mixed-signal products adopt the SGW configuration. The separation for the well ties and supply rails is supplementary if obviously problematic interferences are caused by the substrate coupling in the well and/or by the well-to-substrate coupling. Well noises also have to be considered in variable threshold voltage designs [25]. Because the resistive connections between the bouncing supply/re-

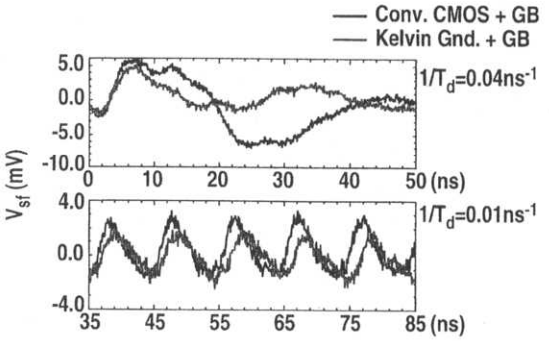

Fig. 17. Attenuated substrate noise waveforms by TCNS-A for $N_{\rm blk} = 12$ in a conventional CMOS design with guardbands, and in Kelvin grounding with guardbands.

turn rails and the well/substrate themselves are eliminated, it can be reasonably effective. However, since the capacitances at a source diffusion (C_{js}) of every MOSFET and also at drain diffusions (C_{jd}) of on-state MOSFETs form parallel and spatially distributed capacitive coupling paths, the guard isolation is degraded and the leakage of the bounce becomes more significant for the higher frequency components.

Another test chip with Kelvin grounding version of TCNS-A [Fig. 5(c)] was tested. Its overall design was the same as the substrate noise evaluation chip. Fig. 17 compares the substrate noise waveforms. The pair of guardbands nearest to the detector is also grounded in order to make comparisons under better noise reduction. The noises are apparently attenuated by using the guardbands compared to the results without using the guardbands under the corresponding conditions given in Fig. 6 and even further by using Kelvin grounding. The maximum $V_{\rm pp}$ reduction of 75% is obtained for the ringing domain ($1/T_d = 0.04$ ns^{-1}); however, the subpeaks remain large ($1/T_d = 0.01$ ns^{-1}) despite the slight attenuation by Kelvin grounding. This is due to the deteriorated isolation by the capacitive coupling. For suppressing the high-frequency components, it is necessary to have methods that work more closely to the substrate noise injection process.

C. Reduced Supply Bounce CMOS Circuits

The universal noise reduction effect can be expected by the suppression of the $V_{\rm dd}$/GND bounces, as deduced from the noise injection processes described in the previous sections. Current steering logic and current mode logic are promising in this sense [26], [27], but increased power consumption as well as the design difficulties are disadvantages. Therefore, we have proposed reduced supply bounce (RSB) CMOS logic, shown in Fig. 18 [21]. This structure can be viewed as a modification of the SGW configuration. A series resistor (Rd) formed by a linear region MOSFET (Md) is inserted between the separated local $V_{\rm dd}$/GND rails and the primary supply/return paths tied to the wells/substrate. Decoupling capacitors (Cd) are also prepared between the $V_{\rm dd}$ and GND rails. This modification is applied locally in every digital block, as shown in Fig. 18(b). Dedicated ground wiring for Cd's is desirable but not absolutely necessary, and without the wiring, the pair of the series Cd's can be reduced to a single large capacitor.

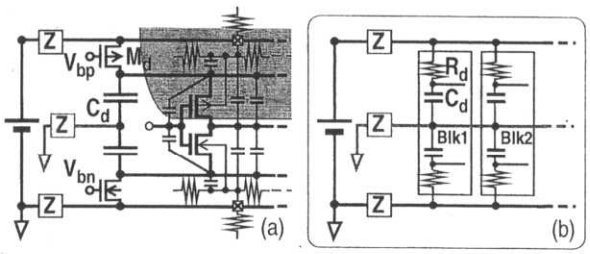

Fig. 18. Reduced supply bounce CMOS circuit configuration. (a) In logic elements. (b) Among subblocks for local supply-current stabilization.

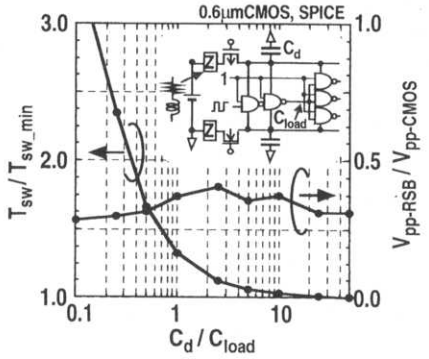

Fig. 19. Substrate noise reduction and switching time increase versus Cd.

The capacitor Cd serves as a local charge reservoir covering the fast logic operations within a digital block and is recharged continuously by the external power source with a time constant of approximately Rd · Cd. Because the largest part of the logic operations is achieved by the charge redistribution, the time constant can be larger than the switching time by several times without lowering the operation speed and typically is set to several nanoseconds. The resultant current flowing through Rd is well flattened, and the bounces on local $V_{\rm dd}$/GND rails are well suppressed. This effect involves only small sensitivity to the size of Rd as long as the above condition is met. Moreover, the local current stabilization in each logic block also reduces the change in the power supply currents flowing in the primary supply/return paths and suppresses the voltage variations on these paths due to interaction with Z_d, Z_g. This remarkable effect contributes to the substrate noise reduction and is well sustained even if the number of reduced noise logic blocks increases in the large-scale designs. The size of Cd must be large enough to cover the logic activity within the block in order to suppress the voltage drop on $V_{\rm dd}$/GND rails to a level sufficiently smaller than the logic amplitude. SPICE simulation results for the dependence of the substrate noise intensity and the switching time increase with the size of Cd (relative value against $C_{\rm load}$) for three-fanout two-input NANDs are shown in Fig. 19. The peak noise amplitudes are reduced to less than 40% compared to the conventional CMOS design and are less dependent on the size of Cd. On the other hand, the increase in switching time ($T_{\rm sw}$) can be less than 5% if a design border is drawn where the ratio of Cd to $C_{\rm load}$ is more than 5.

Note that the collective capacitances parasitic to the local $V_{\rm dd}$/GND rails among inactive logic elements work as the charge reservoir, equivalent to Cd. Equal noise reduction with

TABLE I
SIZES OF Cd IN TEST CHIP

	C_d [A]	C_d [B]
RSB(1)	5pF	—
RSB(2)	10pF	5pF
RSB(3)	15pF	10pF

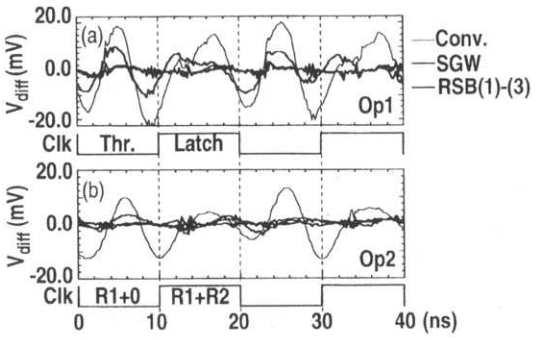

Fig. 20. Measured substrate noise waveforms by test circuit in conventional CMOS, SGW-CMOS, and RSB-CMOS configurations. (a) In Op1 at clock frequency of 50 MHz. (b) In Op2 at 100 MOPS.

almost no increase in switching time can be expected for logic blocks with average activity of less than 20%, even without providing the additional capacitor Cd.

In applying the RSB-CMOS, no design modifications are required at either the gate-level schematic or the layout if standard cell libraries support SGW-CMOS. It is only necessary to place sets of Md and Cd to power bars in the digital blocks designed with established synthesis and place-and-route CAD tools. Using a high-resistivity poly-Si for Rd's and/or a double poly-Si or MOS capacitors for Cd's laid beneath the power bars can minimize areal overhead.

The efficacy of the RSB-CMOS circuits was demonstrated. The test chip shown in Fig. 10 has modules with RSB-CMOS as well as those with SGW-CMOS and conventional CMOS for comparison. The RSB-CMOS modules have pairs of Md+Cd provided for each of the digital sub-blocks ([A], [B]) in the test circuit, and the size of Cd is parameterized as in Table I. Measured waveforms under similar conditions with Fig. 11 are given in Fig. 20. Obvious noise reduction is achieved in the RSB-CMOS circuits, and significant portions of the substrate noise remain in the SGW-CMOS circuits, which are found for both of the operations (Op1, Op2). The peak noise intensity for Op2 is smaller than that for Op1 because of the smaller activities in Op2. The SGW-CMOS circuits sustain their effectiveness in Op2 because of better guard isolation achieved by using the stacked MOSFETs in the sub-block [B]. The absolute peak-to-peak substrate noise amplitudes versus the number of active test circuits are summarized in Fig. 21. In contrast to linear increases against $N_{\rm blk}$ found in the conventional CMOS and the SGW-CMOS circuits, the noises in the RSB-CMOS circuits are well suppressed and independent of $N_{\rm blk}$. This distinct property comes from the local supply current stabilization in every logic sub-block and causes a notable difference from the SGW-CMOS circuits with local decoupling capacitors

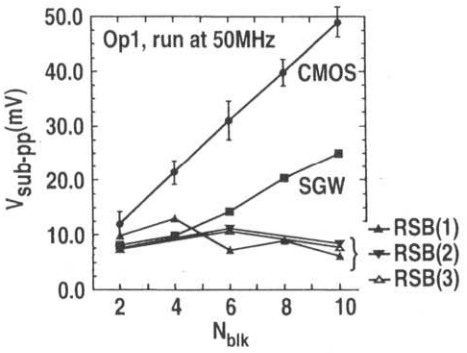

Fig. 21. Measured absolute noise amplitude versus $N_{\rm blk}$.

that can moderately reduce the noise by virtue of the equivalent logic activity reduction. It has also been proved that the capacitive coupled currents directly injected to the substrate make minor contributions to the substrate noise. The differences in effectiveness among RSB-CMOS(1), RSB-SMOS(2), and RSB-CMOS(3) are negligibly small. This indicates that the parasitic capacitances in the inactive logic elements form a local charge reservoir. Note that the order of increasing noise amplitude—RSB-CMOS, SGW-CMOS, and conventional CMOS circuits—is opposite to that of nearness to the detector in the test chip layout, and thus the physical separation does not affect these results. The maximum noise reduction reaches 90% to a CMOS at $N_{\rm blk} = 10$. Further noise reduction can be expected for larger scale digital circuits if the block structuring and activity distributions are optimized.

VI. CONCLUSION

The most dominant process of substrate noise injection in CMOS logic circuits is the leakage of the voltage bounce on the supply/return rails into the substrate. This bounce arises from the interaction of the supply (=return) current with the parasitic impedances on the supply/return paths. The current is formed by charge transfer between the total parasitic capacitances of the logic circuits and an external power source. Logic transition activity determines the amount of charge transfer and thus noise intensity. Substrate noise measurements with 100-μV 100-ps resolution on the transition-controllable noise source and also on the practical CMOS logic circuits clearly prove these observations. A time-series divided parasitic capacitance model is proposed as the supply current estimator for simulating the substrate noise injection. The efficiency and accuracy of the model was well demonstrated by simulations on the logic circuits and by comparisons to the measurement results. The model can be used to optimize the reduced substrate noise design at the circuit level.

Substrate noise reduction techniques were summarized and their efficacy quantified. Traditional guardbands and Kelvin grounding proved to be effective in reducing low-frequency components such as ringing. However, high-frequency components such as peaks reflecting the logic activities were less attenuated due to an increase in parasitic impedances on the supply/return paths and also to a deterioration in the capacitively coupled guard isolation. As is obvious from the noise injection process, the substrate noise can be reduced

by suppressing the return bounce. An RSB CMOS circuit was proposed as a universal noise-reduction technique at the circuit level, and more than 90% noise reduction over that of a conventional CMOS was demonstrated. These results can form the basis of reliable noise management methodologies in mixed-signal IC design.

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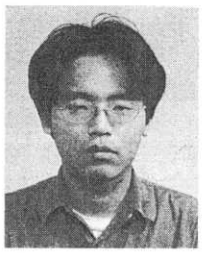

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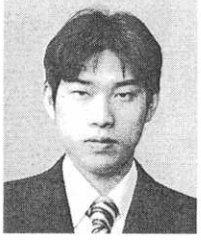

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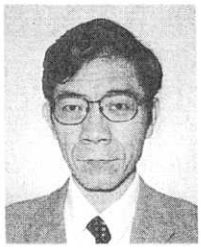

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