Novel TCAD-based Signal-Flow Graph Approaches for the Stability Analysis of Power Semiconductor Devices

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Abstract

Technological innovation in power electronics is desired to realize the social demand for the spread of renewable energy and the promotion of electrification of automobiles to achieve carbon neutrality. Power devices are key components in power electronics, and their performance has been improving. As their performance improves, the occurrence of unstable behaviors such as oscillation and noise in power device packages and circuits can cause system failures. Hence, a new design technology to ensure the stable operation is required. In this study, a novel design method is proposed and applied to oscillation phenomena of SiC-MOSFETs and Si-IGBTs during short-circuit operation. The effectiveness of the method is demonstrated by comparing the results calculated using the proposed method and the results obtained using conventional methods and experimental results.

In chapter 1, the requirements for power semiconductors in the international effort to achieve zero CO_2 emissions in 2050 are summarized. Then, the trend of research and development on the improvement of power device characteristics for smaller and higher efficiency power conversion systems is discussed, focusing on Si-IGBT and SiC-MOSFET.

In chapter 2, previous studies on oscillation phenomena and its suppression are summarized, which can become issues as the power devices are improved. These previous studies can be classified into two categories: one based on equivalent circuits and the other based on device physics. However, there has not been sufficient discussion on the oscillation phenomenon that strongly couples circuits and devices, which is becoming more important as power devices become more high-performance. Technology computer aided design (TCAD) mixed mode simulation can handle both circuits and device physics, however, it is difficult to use it for realistic device design due to the large amount of calculation.

In Chapter 3, a new method based on the S-parameter and the signal flow graph (SFG) is introduced to analyze the circuit stability. This method allows us to calculate the frequency response of the output current to the external field maintaining the response of the carrier distribution and electric field inside the device. The signal gain for the focused operating mode can be easily calculated by applying Mason's rule to the SFG. Additionally, the stability analysis using the Nyquist plot enables not only the judgment of the system

stability with respect to the design parameters but also the quantitative evaluation of the stable/unstable margin.

In Chapter 4, the usefulness of the proposed method is verified by applying it to the oscillation phenomenon of SiC-MOSFETs during Type II short-circuit operation. The S-parameters are calculated from the TCAD model for a commercial SiC-MOSFET, and stability analysis is carried out using the SFG. The dependence of the gate resistance required for oscillation suppression obtained from the mixed mode simulation of TCAD is compared with the results obtained from the proposed method. The agreement between the proposed method and the results of TCAD mixed mode simulation is confirmed. Stability analysis is conducted for both the mode in which a single switching device oscillates by coupling with parasitic elements of the circuit and the mode in which oscillation occurs through switching devices connected in parallel. The characteristics of each mode during short-circuit operation are clarified, and the stability phase diagram in the design parameter space is calculated for each mode by taking advantage of the computational speed. It is shown that which mode becomes unstable depends on the design parameters.

In Chapter 5, the proposed method is applied to the oscillation phenomenon of Si-IGBTs under Type II short-circuit operation and the oscillation mechanism is investigated. Experimental results revealed that the oscillation occurred during Type II short-circuit operation and it can be suppressed by increasing the gate resistance. The resistance required for oscillation suppression decreases as the collector voltage increases. The stability analysis is conducted using the proposed method. It is confirmed that the calculated critical gate resistance decreases as the collector voltage increases. The results are in good agreement with the experimental results. The internal behavior of the device under the oscillation state is also analyzed. During the short-circuit operation, a high electric field region is formed at the boundary between the base and drift layers, and the carrier distribution at both ends of the plasma region is modulated through the electron-hole plasma. This modulation becomes more responsive when the collector voltage is smaller.

In Chapter 6, the development potential of the proposed method and future challenges are discussed.

This study presents a new method for accelerating the development of power devices and power electronics systems that contribute to CO_2 reduction, which is becoming an international effort. This method provides an integrated approach for managing the multi-level design hierarchy, from devices to power conversion systems. It is expected that this achievement will make it possible to fully use the potential of power devices and contribute to expanding the application field of power electronics.

Abstract

再生可能エネルギーの普及，自動車などの電動化を推進するため，パワーエレクトロニクスの技術革新が期待されている．パワーデバイスはそのキーとなる部品であり高性能化が進んでいる．高性能化に伴いパワーデバイスのパッケージや回路で生じる発振・ノイズなどの不安定動作が課題となっている．このような不安定動作はシステムの故障や誤動作の原因となるため，安定動作を担保する新しい設計技術が求められている．本研究ではパワーデバイスの内部動作から回路やシステムまでを統一的に安定化する新たな設計手法を提案する．

第 1 章では，2050 年の CO_2 排出量実質ゼロに向けた国際的な取り組みの中でパワーエレクトロニクスの効率改善，適用範囲拡大に向けた取り組みのまとめを行った．さらに電力変換システムの小型化・高効率化に向けた炭化ケイ素-金属酸化膜電界効果トランジスタ（SiC-MOSFET）とシリコン-絶縁ゲート型バイポーラートランジスタ（Si-IGBT）の高性能化の現状をまとめた．

第 2 章では，パワーデバイスの高性能化に伴い顕在化する発振現象と，その抑制に関する先行研究の到達点を整理した．先行研究は等価回路に基づく研究と，デバイス物理に基づく研究に分類される．しかし，パワーデバイスの高性能化に伴い顕在化する回路とデバイスがより強く結合する発振現象について十分な議論がされていなかった．Technology computer aided design（TCAD）の mixed mode simulation は回路とデバイス物理の双方を取り扱えるが計算量が多く，現実の素子設計への適用は難しく，課題となっている．

第 3 章では，パワーデバイスの内部動作から回路やシステムまでを統一的に設計する手法を提案する．本手法では，デバイスモデルを元に，TCAD シミュレーションの結果から求めた S-parameter と回路を，signal flow graph（SFG）を用いて統一的に取り扱い安定性を解析する．この手法では，デバイス内部のキャリア分布や電界の外場応答を維持したモデル化が可能である．SFG に対して Mason’s rule を適用することで着目した動作モードに対する信号ゲインを容易に計算することができる．安定性解析に Nyquist plot を用いることで，設計パラメータに対する安定・不安定の判定を行うだけでなく，設計者が定量的にマージンを設定することが可能になる．

第 4 章では, 提案手法を SiC-MOSFET の Type II 短絡動作時の発振現象に適用することで手法の有用性を示した．市販の SiC-MOSFET の動作を模擬した TCAD モデルから S-parameter を計算し，SFG を使って安定性解析を実施した．TCAD mixed mode simulation から求めた発振抑制に必要なゲート抵抗の回路パラメータ依存性と提案手法から求められた計算結果を比較し，提案手法と TCAD mixed mode simulation の結果が一致する事を確認した．また，単素子が回路の寄生要素と結合して発振するモードと，並列接続された素子を通じて発振するモードの双方についてそれぞれ安定性解析を実施した．短絡動作時の各モードの特徴を明らかにするとともに，計算速度を生かし，モード毎に設計パラメータ空間内での安定性の相図を計算し，設計パラメータにより不安定になるモードが異なる事を示した．

第 5 章では，提案手法を Si-IGBT の Type II 短絡動作時の発振現象に適用した．はじめに，Si-IGBT の Type II 短絡動作時の発振を実験的に調べ，提案手法による計算結果が実験結果と一致することを示した．また，発振状態でのデバイス内部動作の解析により，短絡動作時にベースとドリフト層境界に，キャリア密度が低下した高電界領域が形成され，外場によってこの領域が伸縮する際，電子正孔プラズマを介して，プラズマ領域両端のキャリア分布が変調されることがわかった．この変調はコレクタ電圧が小さく，高電界領域が狭いほど大きいことが分かった．実験結果の対応から，短絡時に生じる高電界領域とプラズマ領域の外場に対する応答が，外部回路との結合により発振を引き起こすと考えられる．以上のように本手法は，簡易な計算で回路安定性評価とデバイス内部状態解析を同時に行うことができる．

第 6 章では，本研究のまとめを行い，本手法の発展性について述べた．電磁界解析と本手法を組み合わせたモジュール構造最適化などについて触れた．

本論文は，今後国際的な取り組みが高まる CO_2 削減に貢献するパワーエレクトロニクスシステムの開発を加速し，デバイスからシステムまでの全体設計を行うための新しい手法を示したものである．本手法は，これまでその特性を十分に生かしきれていなかったパワーデバイスの特性活用を進め，パワーエレクトロニクスの適用範囲拡大に貢献することが期待される．

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Chapter 1

Overview of power electronics and power semiconductor

1.1 Social demand for power electronics

Global warming is considered as one of the most important and urgent issues for human society. The Paris agreement was an international agreement to limit the temperature increase to less than 2 degrees Celsius compared to pre-industrial levels. The intergovernmental panel on climate change's (IPCC's) 2018 "Global warming of 1.5°C" report [5] states that the average global temperature in 2017 was about 1 degree Celsius higher than it was before the industrial revolution, and that the average temperature increase will reach 1.5°C between 2030 and 2050 if the current rate of temperature increase is maintained.

This report also states that if global warming is limited to 1.5°C, it will be possible to suppress the loss of some ecosystems that would occur with a high degree of certainty if temperatures are allowed to increase to 2°C. This scenario requires a 45% reduction in CO_2 emissions by 2030 and a net-zero level by 2050. International energy agency (IEA) shows a roadmap to reduce CO_2 emissions to NET zero by 2050 [1]. According to the roadmap, 60 percent of global vehicle sales must shift to electric vehicles by 2030, new sales of internal combustion engine vehicles must be ceased by 2035, and renewable energy sources must account for 90 percent of electricity generation by 2050.

This roadmap states that the improvement in power electronics technology will expand its application field and improve the performance of power converters and increase the ratio of renewable energy to total power generation.

Because power electronics handles a wide range of output power, the technology requirements depend on the application field and output power.

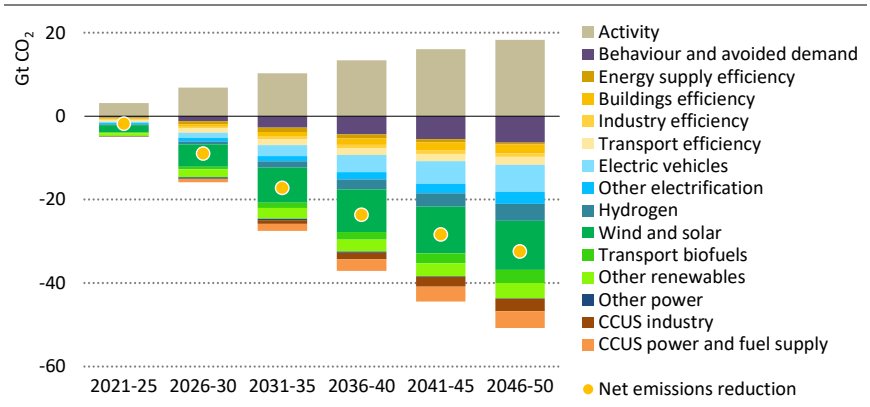


Fig. 1.1 Average annual CO_2 reductions from 2020 in the net zero emission. [1]

For example, in the case of a power converter unit used in a vehicle such as an automobile, downsizing the volume of the converter unit may be more important than other applications. It has been reported that the improved aerodynamic performance of the vehicle body due to the downsized converter contributes to the improved cruising range as well as improved efficiency of the converter [6].

It has also been reported that the use of silicon carbide (SiC) power devices in railroad inverters not only improves an inverter efficiency but also enables power regeneration under the high load operating conditions, thereby reducing the need for deceleration using thermal brakes and improving the overall power efficiency by sharing the regenerated power with other trains [7, 8].

In this way, to expand the field of applications of power electronics, it is necessary not only to improve the efficiency of individual systems components, but also to optimize the entire system in terms of required characteristics, operation, and cost. Therefore, the development of design technology to realize these requirements is an important theme.

1.2 Functions of power semiconductors in power electronics

To realize the requirements for power electronics described in the previous section, it is necessary to improve the characteristics of the power device and the circuit system. Recently, it has been shown that SiC power devices can significantly improve the performance of power devices by achieving unipolar switching devices in the high breakdown voltage region, which could not be achieved with conventional silicon metal-oxide-semiconductor field-effect transistors (Si-MOSFETs). As can be seen from the examples of automobiles and railroads introduced in the previous section, the improvement of power devices can not only reduce the loss of the power devices themselves but also resolve the issues of the power electronics system.

Figure 1.2 shows a circuit diagram connecting a bidirectional chopper circuit and a motor drive inverter. In this circuit, the voltage of the storage battery is boosted by the chopper circuit and it is used as an input to the motor drive inverter. By increasing the voltage, it becomes possible to reduce the current required to drive the motor, which enables the wiring and motor to be smaller and lighter. The bidirectional chopper can also charge the storage battery during regeneration from the inverter.

Although the output of the chopper circuit is desired to be constant, it has a finite ripple due to the switching of the FETs. The ripple current δi_L is proportional to $\frac{T}{L}(V_{in} - V_{out})$, where V_{in} and V_{out} are the input and output voltages, T is the switching period, and L is the inductance. Therefore, the switching frequency is inversely proportional to the inductance L when the ripple current is to be suppressed to a particular value.

Generally, the volume and weight of the inductor increase with the inductance. Therefore, by increasing the switching frequency, it becomes possible to reduce the size of the inductor and filter capacitor, which occupy a large proportion of the weight and volume of the power conversion unit. However, an increase in the switching frequency increases the switching loss of the power devices. Therefore, it is important to reduce the switching loss to downsize the power conversion system.

In a three phase inverter circuit, two switching devices like as insulated gate bipolar transistors (IGBTs) or FETs, are connected in series for each phase (U, V, and W), and a diode such as a PiN diode or SBD is connected in parallel with each switching device. In some cases, the parasitic diodes of the MOSFETs are used instead of connecting the diodes in parallel. In the inverter circuit, the motor is rotated by switching the gate signals of the U, V, and W phases. When the gate signal is switched off, the current is diverted from the FET

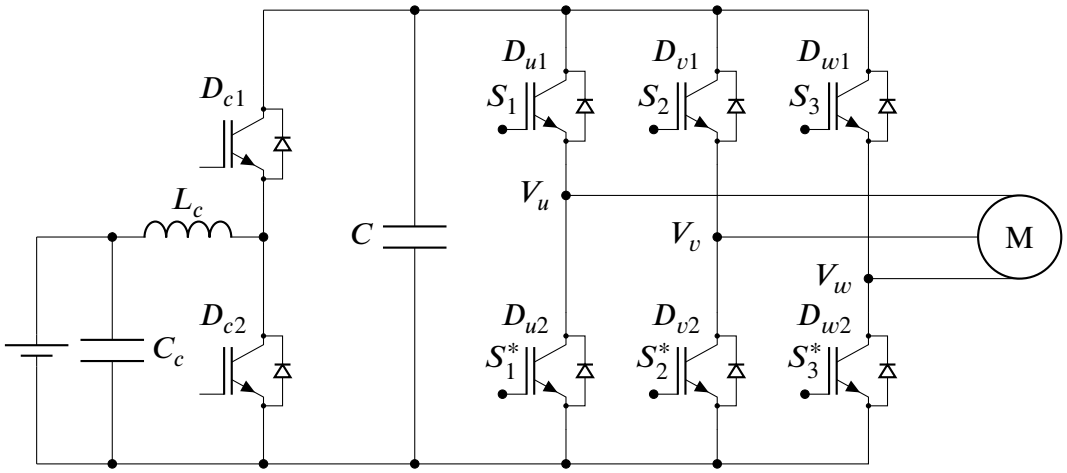


Fig. 1.2 Circuit diagram of a three phase inverter.

to the reverse side diode. For this reason, the diode is required in parallel with the switching device.

In addition to efficiency during normal operation, power converters must prevent the failure of components triggered by a failure of another component. Normally, if an excessive voltage or current flow is applied, the controller sends an off signal to the power devices to protect them. Therefore, power devices must have tolerant before entering the protective operation. For example, if the load is short-circuited during the switching operation, the device must be able to withstand high voltage and high current for several microseconds to safely cut off the current flowing through the device.

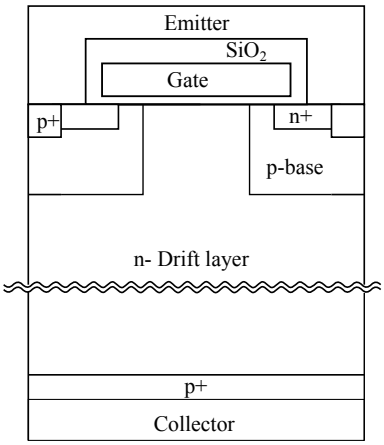
1.3 Power semiconductor devices and their trends

In this section, the trends of technological development in power devices are discussed, focusing on Si-IGBT and SiC-MOSFET.

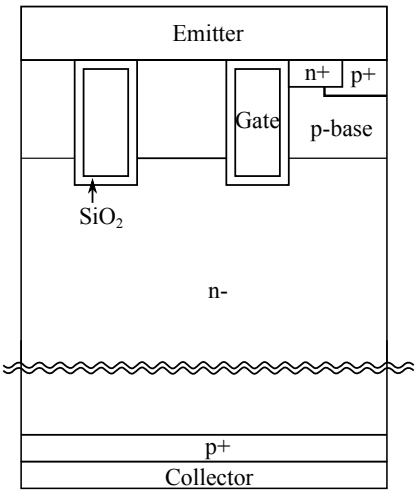
1.3.1 Silicon insulated gate bipolar transistor

Si-IGBTs have been developed to realize both MOSFET-like usability of voltage driving and the characteristics of bipolar transistors, such as high current capability, wide safety operating area and short-circuit tolerance, in contrast to the gate-turn off thyristors (GTOs), which were the mainstream until IGBTs were developed. The device structure is shown in Figure 1.3(a). The structure consists of a bipolar transistor connected to a MOSFET in series. This structure allows the device to handling higher current than ordinary MOSFETs and simpli-

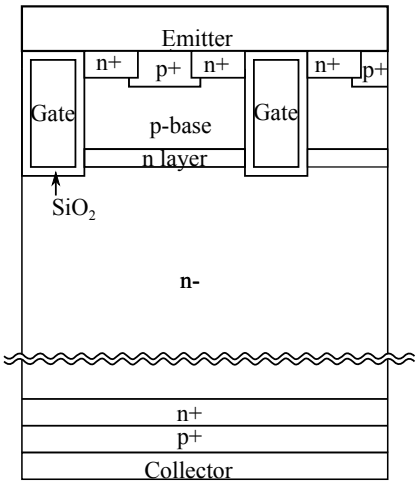
fies the control circuits compared to ordinary bipolar devices. In this subsection, the trends in the development of IGBTs are discussed [9].



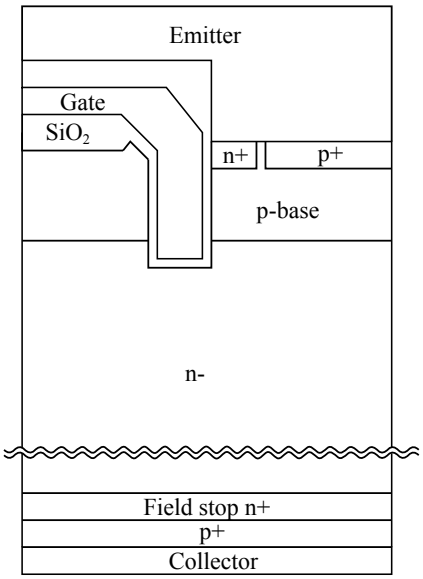
(a) Insulated gate bipolar transistor (IGBT).



(b) Injection enhanced gate transistor (IEGT).



(c) Carrier stored trench-gate bipolar transistor (CSTBT).



(d) Trench field-stop IGBT.

Fig. 1.3 Schematics of insulated gate bipolar transistors.

IGBT structures were proposed in the late 1970s and early 1980s. Baliga et al. proposed an insulated gate rectifier (IGR) with a p+ region on the back side of the MOSFET [10]. This device had the problem of low latch-up tolerance of the parasitic thyristor when a large

current was applied. Nakagawa's non latch-up IGBT structure solved this problem [11]. They showed that the latch-up can be suppressed by omitting the source contact area in the horizontal direction. This structure led to the widespread use of IGBTs in power supply circuits with high voltage and high current.

As there is a trade-off between the on-voltage and the switching characteristics, how to improve this trade-off relationship has been the history of IGBT development. To reduce the on-voltage of IGBTs, the cells were miniaturized, and trench-gates were developed. In the process of increasing the breakdown voltage of these trench-gate IGBTs, there was the problem that the on-voltage could not be reduced sufficiently. This problem was solved by the injection enhancement (IE) effect. The IE effect is achieved by reducing the number of emitters in the trench-gate IGBTs, which reduces the extraction of holes from the emitters during conductivity modulation and increases the carrier concentration on the surface side. This structure enables a reduction in on-voltage even in high voltage devices [12].

A carrier stored trench-gate bipolar transistor (CSTBT) has also been reported [13]. The CSTBT has a high concentration n layer on the surface side of the device, as shown in Fig. 1.3(c), based on the same concept as the IE effect. This region reduces the efficiency of hole extraction from the emitter side.

The structure of the drift layer has also been improved. Initially, epitaxial growth was performed on the p-substrate to provide a junction. Additionally, the design was optimized by controlling the lifetime of holes due to the trade-off with switching loss (punch-through: PT-IGBT). Goodman et al. proposed an n+ buffer structure. By adding the n+ buffer region on the back side with a higher concentration than that of the drift layer, the trade-off between on-voltage and switching speed can be improved by controlling the lifetime [14].

Later, using a thin-wafer process, the non punch-through (NPT) structure was proposed to reduce the injection efficiency from the p-collector layer without lifetime control [15]. In contrast to the conventional drift layer formed by epitaxial growth on a Czochralski (CZ) wafer, the NPT-IGBT uses a floating zone (FZ) wafer and forms a backside p-structure using a thin-wafer process. In this process, the injection efficiency from the p-collector is reduced so that the lifetime control is not applied.

This design allows us to reduce the carrier injection concentration on the backside compared to conventional PT-IGBTs and to flatten the carrier concentration in the entire drift layer during conductivity modulation. This makes it possible to increase the contribution of the electron current to the total current, thus lowering the drift layer resistance with a smaller carrier concentration.

As a further improved concept to the NPT-IGBT, a field stop (FS) structure IGBT was proposed to reduce the n-drift layer thickness in order to lower on-voltage and to stop the depletion layer reaching the back side [16].

After that, optimization of the surface structure, drift layer, and back surface structure have been carried out, and IGBTs with various breakdown voltage ranges from 1.2 kV to 6.5 kV are used in various application fields, including home appliances, automobiles, trains, and grid power conversion devices.

1.3.2 Silicon carbide metal-oxide-semiconductor field-effect transistor

Physical properties of silicon carbide

As described in the previous section, IGBTs have played a major role in the field of power electronics as high-voltage and high-current switching devices. Although many studies have been conducted to improve their performance, there is a limit to the switching speed because they are bipolar devices. In recent year, silicon carbide metal-oxide-semiconductor field-effect transistors (SiC MOSFETs) have attracted attention as devices that overcome the limitation of Si-IGBTs.

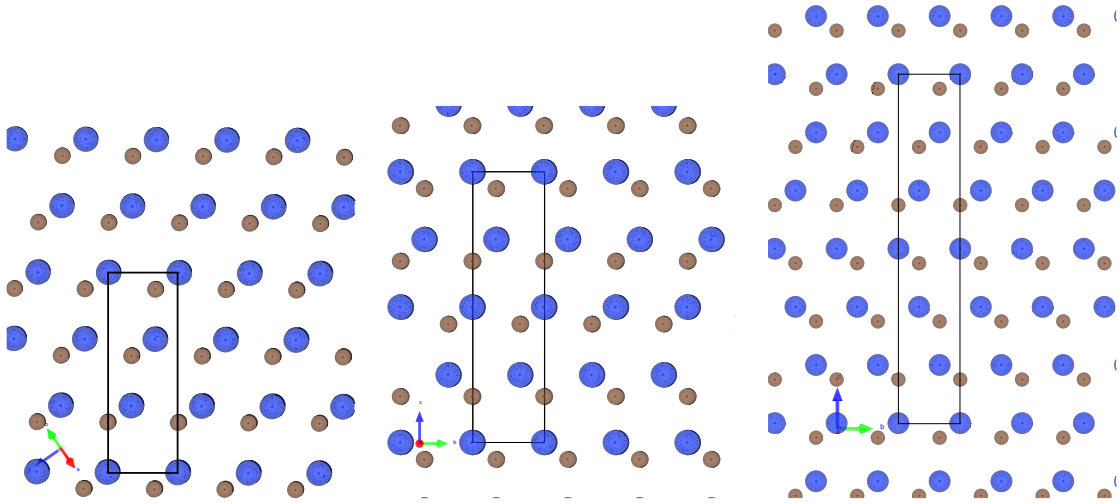
SiC is a semiconductor material of which the band gap is three times larger than that of silicon. It has a higher electric field for breakdown than Si. Therefore, it is possible to reduce drift layer resistance by increasing the drift layer doping concentration and thinning the drift layer thickness. It is theoretically possible to reduce the drift layer resistance to about 1/1000 of that of a Si device with the same breakdown voltage [17].

	Silicon	3C-SiC	4H-SiC	6H-SiC
Energy Band Gap [eV]	1.12	2.23	3.26	3.02
Critical electric field for breakdown [MV/cm]	0.3	1.5	2.8	3.0
Thermal Conductivity [W/cm K]	1.5	4.9	4.9	4.9
Electron mobility [cm^2/Vs]	1350	1000	1000 ($\perp$ c) 1200($\parallel$ c)	450 ($\perp$ c) 100 ($\parallel$ c)

Table 1.1 Comparison of material properties of Silicon Carbide poly types and Silicon [3, 4].

Incidentally, SiC has many polytypes. The atomic configurations of 3C, 4H, and 6H-SiC are shown in Figure 1.4. Table 1.1 shows the physical properties of each polytype. The band gaps of 4H-SiC and 6H-SiC are larger than that of 3C-SiC, and they have a higher breakdown electric field. In addition, Baliga's figure of merit of 4H-SiC is better than that of

6H-SiC because the electron mobility of 4H-SiC is higher than that of 6H-SiC. As shown in Fig. 1.4, 3C-SiC, 4H-SiC, and 6H-SiC have a repeating structure of silicon and carbon atom pairs with 3, 4, and 6 cycles in the stacking direction [2]. Stacking faults are easily generated by the fluctuation between other polytypes during the crystal growth process. In particular, 3C-SiC is steady state at epitaxial growth temperature and other polytypes can change into 3C-SiC during epitaxial growth. To solve this problem, step-flow epitaxial growth has been proposed, in which an off-angle is applied to the SiC bulk substrate. This method enable the crystal growth maintaining the repetitive structure of the crystal [18]. Although the advent of this method has enabled high-quality epitaxial growth, the number of epitaxial defects is larger than that in Si, and it is an ongoing challenge to reduce defects during crystal growth and improve its quality.



(a) 3C-SiC (b) 4H-SiC (c) 6H-SiC

Fig. 1.4 Cristal structures of silicon carbide poly types [2].

Basal plane dislocations (BPDs) and stacking faults are important factors in the crystal quality of SiC. There are many threading screw dislocations (TSDs), threading edge dislocations (TEDs) and BPDs generated during crystal growth in 4H-SiC available in the commercial market today. During epitaxial growth, most of the BPDs are converted to harmless TEDs in the buffer layer. A few BPDs, however, are inherited in the epitaxial layer. Some of the BPDs change into stacking faults due to the recombination energy of electrons and holes injected into the epitaxial layer when the device operates in a bipolar mode. The expand of the stacking faults causes degradation of the conductivity of the epitaxial layer. Therefore, the operation of body diodes in MOSFETs can induce the degradation as well as bipolar devices such as PiN diodes. To solve this problem, it has been proposed to place another epitaxial buffer layer between the bulk substrate and the drift layer with a higher doping

concentration [19]. This buffer layer can suppress the injection of holes and the expansion of stacking faults.

Since the material properties of SiC can improve the trade-off between breakdown voltage and specific on-resistance $R_{on}A$, unipolar devices can be used in the voltage range where bipolar devices have been used. SiC-MOSFETs have been reported in the breakdown voltages range from 650 V to 10,000 V.

One of the features of SiC is that the MOS interface can be formed by thermal oxidation. However, the SiC/SiO_2 MOS interface has more defects than Si, and the effective invertinon channel mobility is lower than the bulk mobility, so improving the interface quality of SiC-MOSFETs has been an important problem since the beginning of SiC device development. The improvement of MOS interface on SiC has been reported in many studies [20, 21]. It has been reported that nitridation of the MOS interface improves the mobility of SiC, which is less than 10 cm^2/Vs using conventional dry oxidation [22–24]. It has also been reported that MOS channels on the carbon-, a-, and m-faces with respect to the silicon-face can improve the inversion channel mobility to 100 cm^2/Vs [20, 21].

In particular, since the a- and m-planes correspond to the perpendicular directions of the surface of SiC, these surfaces can be used to form channels for trench MOSFET structures. In addition, it has been reported that the channel mobility is greatly improved by using the (00−38) plane [24].

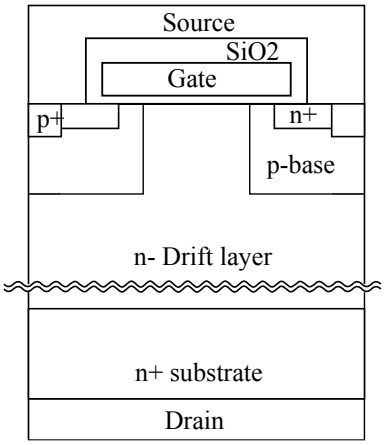
One of the solutions to the high channel resistance is to increase the channel density in the device structure. In particular, for 650 V and 1.2 kV class devices, the ratio of the channel resistance to total device resistance is high, the reduction of the cell pitch is effective in improving the channel density.

Vertical structures are the main type of SiC power MOSFETs being developed. The two different channel structures, planar and trench gate have been developed. Although the high critical electric field for the breakdown is the one of the advantage of SiC, the high electric field at pn junction increases the electric field on the gate oxide film of the MSOFETs. The high electric field causes breakdown and the decrease in lifetime of the gate oxide. Therefore, reducing the electric field of the gate oxide is an essential design topic for SiC power MOSFETs that require high reliability. Although silicon trench MOSFETs can achieve low ON-resistance due to the absence of JFET resistance, SiC-MOSFETs require a JFET-like structure to reduce the electric field of the oxide film.

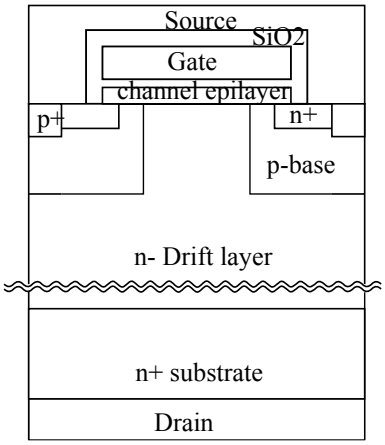
Planar MOSFET

In the planar SiC MOSFET, the channel and source regions are formed under the gate oxide film on the semiconductor surface, similar to the planar structure of Si, as shown in Figure

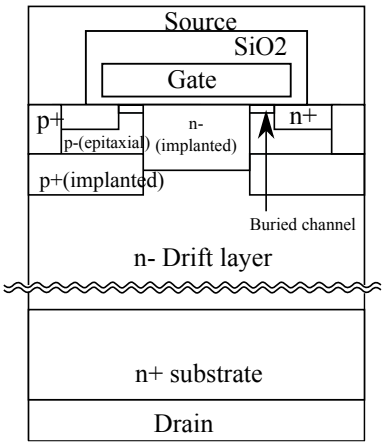
1.5(a). On the other hand, it is difficult to form channels by impurity diffusion through an activation annealing because of low diffusion coefficient of impurities in SiC. To activate the implanted impurities, an activation annealing of 1500-degree C or higher is needed. Hence, a different process is required such as the formation of a gate oxide film after the activation annealing.



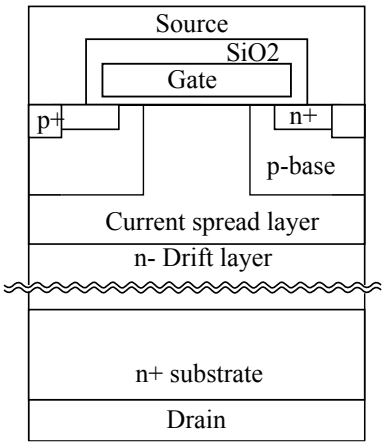
(a) Planar MOSFET



(b) SiC MOSFET with channel epitaxial structure [25]



(c) IEMOSFET [26].



(d) SiC MOSFET with current spreading layer. [27]

Fig. 1.5 Schematics of Silicon Carbide MOSFETs.

Shortening the channel length and shrinking the cell pitch is effective for reducing the channel resistance because of the low MOS channel mobility of SiC [25]. Palmour et al. have reported on planar MOSFETs in the 900 V to 15 kV range [28]. In this paper, the specific on-resistance of the planar MOSFET for a 1620 V device was reported of 2.7 $m\Omega cm^2$.

In comparison in the channel mobility between ion implantated p-base and epitaxial grown p-base, the channel mobility on the latter is higher [29]. Implanted and epitaxial

MOSFET (IEMOSFET) is proposed [30] as shown in Fig. 1.5(c). IEMOSFET is a planar MOSFET that is fabricated by forming an ion implantation region at the bottom of the p-base, followed by p-type epitaxial growth to form the channel region, and N-type implantation to form the JFET region. The low-mobility channel can be improved using a buried channel [31]. DIOMOS with the buried channel not only reduces channel resistance by improving the channel mobility but also suppresses a bipolar operation by optimizing the epitaxial channel structure [32].

The MOS channel on carbon-face can achieve several times higher mobility than that of Si-face. Using this property, DIMOSFET on the carbon-face can improve the trade-off between $R_{on}A$ and breakdown voltage [26, 33].

The JFET resistance can be reduced by adding a current spreading layer with higher impurity concentration than that in the drift layer (see Fig. 1.5(d)). By applying this structure, the trade-off between on-resistance and breakdown voltage can be improved [27].

Trench MOSFET

The SiC trench MOSFET enables the channel length and cell pitch reduction. It can use the channel on a-plane and m-plane, which have higher mobility than that of silicon-face.

To reduce the electric field of the gate oxide of trench MOSFETs, various structures have been proposed. One of these is the double trench structure [34]. In this structure, trenches are formed across the gate trench and p-type regions are formed on the trench side wall using ion implantation. SiC-MOSFETs with the double trench structure show 1260 V breakdown voltage and 1.41 $m\Omega cm^2$ whereas the planar MOSFETs show 2.3 $m\Omega cm^2$ [34]. A significant improvement in characteristics have been achieved for 1.2kV class SiC MOSFETs with the double trench structure.

In another structure, a p-type region is formed at the bottom of the gate trench. The trench MOSFET with the bottom p-well structure has achieved 2.15 $m\Omega cm^2$ with 652 V breakdown voltage [35] and 1.19 $m\Omega cm^2$ with 1080 V break down voltage (this report excludes the substrate resistance) [36]. In the bottom p-well structure, if the bottom p-well is not connected to the source region, the avalanche tolerance decreases [37]. Therefore, it is necessary to connect the bottom p-well to the source region. However, due to the low activation rate of p-type impurities in SiC, the sheet resistance of the p-region is high, and it is necessary to provide a connection region to the source electrode at certain intervals, and optimization of these region is important in the viewpoint of reducing R_{on} [35].

An asymmetric trench structure has been proposed. In this structure, the p-type region protecting the bottom of the gate oxide film is directly connected to the source region. The gate oxide electric field is suppressed by the asymmetric p-type region surrounding the gate

trench. Although there is a disadvantage that half of the gate channel is disabled, 3.5 mΩcm^2 has been achieved in a 1.2 kV class device. It can also operate stably during avalanche breakdown [38].

TEDMOS that reduces channel resistance by increasing channel density and channel mobility through the formation of trenches in the channel region has been reported [39].

A V-groove-type trench MOSFET of which channel is formed on the (03−38) plane has been proposed because the channel mobility on the crystal plane is higher than that on the (0001) plane [40, 41]. In order to mitigate the electric field at the bottom of the V-groove gate structure, a structure with a thicker oxide film and an embedded p-structure to reduce the electric field has also been reported [42].

Super Junction

In SiC MOSFETs, while the reduction of channel resistance has been the focus of technological development for a long time, the reduction of drift layer resistance has also been studied recently. In particular, the development of the super junction (SJ) structure, which is used in Si power MOSFETs, has progressed rapidly in recent years. Kosugi et al. have been reported that SiC-SJ structure can exceed the SiC limit by experiment [43]. In this study, a 5.5 μm SJ structure was fabricated by two repetitions of MeV-accelerated ion implantation and epitaxial growth. The TEG showed a breakdown voltage of 1545 V and a drift layer resistance of 1.06 mΩcm^2 was obtained.

By combining the trench structure and SJ structure, 3.2 mΩcm^2 was achieved at a breakdown voltage of 1500 V [44]. Although the absolute value of $R_{on}A$ is comparable to that of conventional structures, it has been reported that the temperature dependence of R_{on} can be reduced by adopting the SJ structure. A combination of SJ and V-groove structures can achieve $R_{on}A = 0.63$ mΩcm^2 and $V_{bd} = 1170$V [45]. Additionally, devices that exceed the SiC limit have been reported, such as a 6kV-class device with multi-epitaxial growth. The SJ structure is expected to be applied to devices up to 10 kV in the future because unipolar devices with high breakdown voltages are effective in taking advantage of the potential of SiC. For practical use, the cost increase due to multiple epitaxial growth is an issue. Epitaxial backfilling technology is also being studied [46], however, breakthroughs related to anisotropic growth conditions and doping concentration control, and improvements in process technology are desired in the future.

Summary

Figure 1.6 shows the trade-off relationship between $R_{on}A$ and V_{bd} for MOSFETs and the theoretical limit for 4H-SiC [47]. The square represents the planar type, the triangle represents the trench type, and the circle represents the trench SJ type. At high voltages, the effect of the channel resistance is small, so the values are close to the SiC performance limit, while the increase due to the channel resistance is not negligible in the 600 V to 1200 V region. The trench structure has a higher potential than planar MOSFETs due to the effect of channel resistance reduction. Additionally, the SJ structure has been reported to exceed the SiC limit in recent years, and is expected to be commercialized in the future.

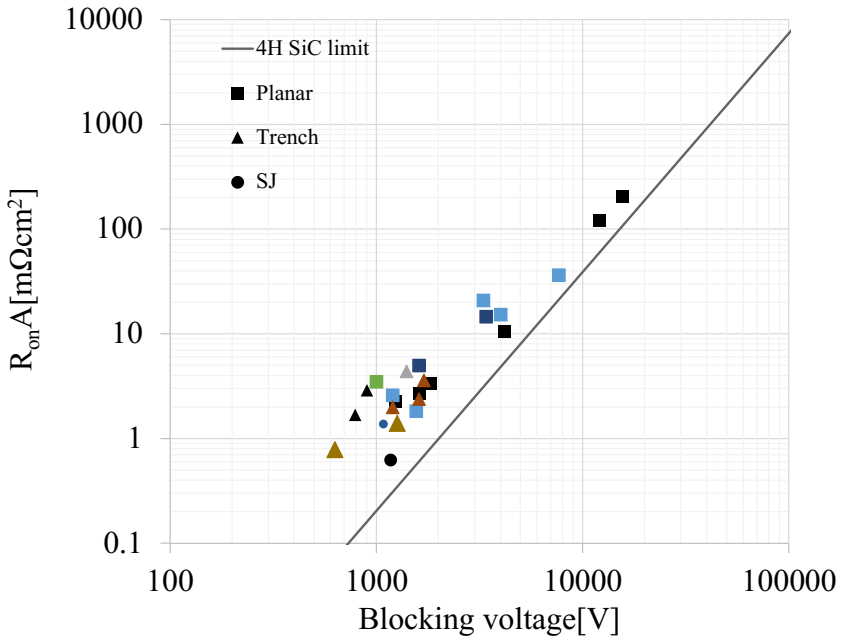


Fig. 1.6 The trade-off relationship between $R_{on}A$ and V_{bd} of SiC MOSFETs.

1.4 Summary

In this chapter, the history and the latest topics of the development of power device technologies are summarized, which are increasingly demanded by society to achieve zero CO_2 emissions by 2050. In particular, the trends in the research and development of Si-IGBT and SiC-MOSFET are summarized. The characteristics of Si-IGBTs have been improved by optimizing the carrier distribution in the drift layer to reduce the switching loss, which is a trade-off between the reduction of conduction loss by the bipolar operation. Addition-

ally, SiC-MOSFETs have enabled high breakdown voltage and low on-resistance by taking advantage of their high breakdown electric field, however, the high breakdown electric field in the semiconductor increases in the electric field of the gate oxide on SiC surface. Hence, the structure of the device must be designed to reduced the electric field of the gate oxide. Various structures have been proposed to achieve both reliability and low ON-resistance. This chapter summarizes the research on Planar, Trench type MOSFETs and SJ-MOSFETs.

Chapter 2

Oscillation phenomena in power semiconductor operation

As the application field of power electronics expands, it has become important to ensure the stable operation of the power devices under various operating conditions. In this chapter, the oscillation phenomenon, which is one of the most important issues for the stability of the power converter systems, is discussed. The oscillation on the device not only causes the destruction of the power device but also radiation noise. For this reason, the mechanism of the oscillations and how to prevent it have been studied from various aspects. In the conventional approaches, devices, packages, control circuits, and power circuits were designed individually. And focuses were optimization for their connection at the design phase of a power conversion system.

As the performance of power devices improves, however, individual optimization at each design phase does not allow to use the full potential of the device due to the accumulation of margins for characteristic fluctuations among components, response delay and reliability. To utilize the benefits of the performance-improved power devices, device, package, control circuit, and power circuit design parameters must be optimized simultaneously to prevent undesirable oscillation.

The major issues discussed for Si-IGBTs and SiC-MOSFETs are

- Ringing and oscillation during turn-on and turn-off in single device operation of Si-IGBTs,
- Ringing and oscillation phenomena during turn-on and turn-off of Si-IGBTs connected in parallel,
- Ringing and oscillation during turn-on and turn-off in single device operation of SiC-MOSFETs,

- Oscillation and ringing during turn-on and turn-off of SiC-MOSFETs connected in parallel,
- PETT oscillation at turn-off of Si-IGBTs,
- Oscillation during short-circuit operation of Si-IGBTs and Si-MOSFETs.

In this chapter, previous studies that investigated these oscillation phenomena will be reviewed.

2.1 Circuit oriented oscillation

Si-IGBTs and SiC-MOSFETs work as amplifiers in power conversion circuits, and change the collector/drain current and voltage depending on the gate voltage. Additionally, MOSFETs and IGBTs have feedback paths from the output to the input side because of their own parasitic capacitances (feedback capacitance, input capacitance, output capacitance), parasitic inductances and capacitances of the package. If the transfer functions of these feedback loops become unstable, the devices can cause oscillation.

When several switching devices are connected in parallel, the feedback signal may be returned to the gate via the devices connected in parallel [48, 49]. This feedback causes oscillation and ringing of output voltage and current of switching devices such as IGTBs and MOSFETs [50–52].

These oscillation and ringing sometimes destruct the power devices, and even if they do not, they increase the loss of power converter and cause EMI. Therefore, it is necessary to suppress these oscillation and ringing. Then oscillation phenomena in various operating conditions, such as turn-on, turn-off, and short-circuit operation, have been studied [51–57].

Oscillation phenomenon in the hybrid module in which Si-IGBT and SiC-SBD are connected in parallel, during a turn-on operation has been reported [51]. It has been reported that the presence of the oscillation was determined by the gate resistance and parasitic inductance of the Si-IGBT and capacitance of the SiC-SBD. Then it was necessary to reduce the parasitic inductance of the module in order to suppress the oscillation without increasing the device loss [51].

In SiC-MOSFETs, self-sustained oscillation during switching operation has been reported [53, 56, 58]. It is shown that several feedback paths can cause the self-sustain oscillation [58]. The drain and source inductance, gate resistance, and the ratio of drain capacitance to gate capacitance are an important parameter to understand the self-sustained oscillation [56].

2.2 Device oriented oscillation

In this section, the oscillation phenomena caused by the internal characteristics of the power devices will be discussed.

Si-IGBTs connected in parallel show a current oscillation between the IGBTs at high collector voltage condition [59]. In order to analyze this oscillation phenomenon of IGBTs, negative gate capacitance has been proposed as an oscillation mechanism [59, 60]. The existence of negative gate capacitance is shown by device simulation using TCAD based on the derived equivalent circuit, and then the stability of oscillation is analyzed analytically.

In IGBTs, plasma extraction transit time oscillation (PETT oscillation) is sometimes observed during a turn-off [61–63]. This phenomenon causes the oscillation of tens to hundreds of MHz in the current and voltage during the tail current flow during the turn-off of the IGBT.

This phenomenon is caused by a negative resistance due to the transfer delay of holes injected from the electron-hole plasma edge to the source electrode [61]. A packet of holes injected from the electron-hole plasma boundary at a certain time moves through the depletion layer over a certain amount of time, and the oscillation frequency can be estimated from the migration speed v_s and the depletion layer width W.

$$f = \frac{3v_s}{4W}. \tag{2.1}$$

In order to estimate the specific charge transfer, information on the depletion layer, electron and hole plasma states at the external voltage in the oscillating state is required. For this reason, TCAD transient simulation has been used to simulate the internal state of the device when the external voltage is modulated near the oscillation frequency. This method has been used to estimate the chip-to-chip oscillation state [62], and to estimate the oscillation state inside the module [63].

Particularly in bipolar devices such as Si-IGBTs, impact ionization is caused by an increase in the electric field in the drift layer during the turn-off, and this can lead to a continuous oscillation phenomenon. This is known as impact ionization avalanche transit time (IMPATT) oscillation, and its suppression is one of the important themes in IGBT [64–66].

2.2.1 Oscillation phenomena in short-circuit operation

Stable operation of power devices during the short-circuit (SC) protection is an important theme. The stable operation of Si-IGBTs and SiC-MOSFETs under SC type I , II, and III conditions has been studied [67–70].

The di/dt during SC type I is determined by the switching device itself, while that of SC type II is determined by the parasitic inductance of the short-circuit loop and the DC link voltage [69]. Therefore, the peak value of SC type II current becomes larger than that of SC type I due to the increase in the gate voltage caused by the displacement current. The experimental waveform shows that oscillation occurs during SC type II [69].

The oscillation between parallel-connected IGBTs during turn-on has been reported [57].

2.3 Conventional approaches to solve the problem and their limit

In order to understand these oscillation phenomena, various studies have been reported on the derivation of equivalent circuits and the analysis of oscillation on the equivalent circuits. There are three major approaches to deriving the equivalent circuit.

The first approach is to determine the circuit parameters of the equivalent circuit by fitting the experimental results. Parameters such as parasitic inductance are determined to reproduce the changes in voltage and current during switching in the experiment.

The second approach is to determine the parameters based on actual measurements. For the measurements, a method using impedance and S-parameter measurements have been proposed [53, 71, 72]. In the method using impedance measurement, the parasitic parameters of each signal terminal are assumed to be the series parasitic parameters of the LCR and calculated from the results of terminal-to-terminal impedance measurements [53]. To improve the precision and accuracy of the measurements of the circuit parameters, a measurement technique using S-parameters has been proposed [71, 72]. This method can avoid the precision degradation caused by the coupling between the floating terminal and the ground when measuring the impedance of power devices. The package impedance can be calculated from the measurement results of each combination of the module terminals, and the S-parameter measurement can be used to model the internal parameters of the package more accurately and easily than the conventional impedance measurement.

The third approach is to calculate the equivalent circuit model based on simulation, which generally uses the finite element method and electromagnetic field analysis [73]. In this method, self and mutual inductance and resistance of copper patterns, terminals, bonding wires and bus-bars are calculated in some current flow conditions.

Once the equivalent circuit is obtained, the operating conditions are analyzed. Several methods are used for this analysis, including the method for determining the time dependence by analytical calculation of small-signal equivalent circuits, the method for perform-

ing stability analysis analytically from the frequency dependence [48, 49], and the method of determining the stable circuit parameters by calculating the time-dependent waveform and frequency dependence using SPICE simulation [49].

In these approaches, MOSFET or IGBT chips are treated as a small-signal model. The small-signal models of the power devices are calculated by parameter fitting to the measured curve forms or simulation calculated curve forms [49].

The other approach is to use technology computer-aided design (TCAD) tools for time-dependent simulation. TCAD simulation using mixed-mode techniques can compute time-dependent behavior of the devices and circuits simultaneously. This is a useful method to compute oscillation phenomena [67, 74]. However, this method has limited applications because it is difficult to converge to the correct state near the oscillation state and the CPU time tends to be long.

2.4 Objective of this study

Oscillation phenomena can be caused by the switching devices with the connected circuits and the internal behavior of the devices. In the conventional approach, circuits and devices are discussed separately, and the phenomena caused by the combination of the both cannot be fully discussed.

As shown in this chapter, ensuring the stable operation of IGBTs and MOSFETs has been a longstanding issue in power devices, and various studies have been conducted. TCAD simulation is a powerful tool for understanding the oscillation phenomena because it can calculate the internal state of the device and the behavior of the circuit simultaneously. However, it requires a large amount of computational time, and its use is limited for parameter optimization. Generally, the device model is replaced by an approximate small-signal model, and then the parameters are optimized by SPICE simulation or analytical calculation.

Additionally, the coupled analysis with the internal simulation of the device requires a large amount of computation time. Although it is possible to analyze the origin of the oscillation phenomenon, the computation cost is too large to optimize the devices and circuits design parameters.

The purpose of this study is to develop a method for parameter optimization based on the TCAD simulation results. This will provide a unified method for the optimization of devices and circuits, and contribute to the realization of technology that can maximize the characteristics of power devices.

2.5 Summary

In this chapter, the oscillation phenomenon and mechanism of Si-IGBTs and SiC-MOSFETs are reviewed. The methods on analyzing these physical phenomena are also summarized. In this study, a novel design method is proposed to discuss the oscillation phenomena by incorporating the internal behavior of the device and circuit parameters.

Chapter 3

Theory of oscillation analysis with a signal flow graph and a scattering parameter

In this study, an analysis based on a scattering parameter (S-parameter) is proposed to treat the oscillation phenomena as discussed in the previous chapter. Impedance measurements of devices and circuits are generally difficult at high frequency because open and short calibration measurements are difficult at high frequency. S-parameter solves this difficulty in high-frequency measurements by using a characteristic impedance termination. Additionally, once the frequency dependence of a circuit element is determined, the internal behavior of the circuit element can be treated as a black box. It is possible to handle from the internal operation of the switching devices to the operation of the circuit system. In this chapter, the general treatment of the S-parameter is briefly described, and then the theoretical method for calculating the oscillation condition based on a TCAD device model is discussed.

3.1 General theory of Scattering parameter (S-parameters)

The figure 3.1 illustrates a multiport network with incident power waves and reflected power waves at its ports.

The incident power waves of i-th port is defined as

$$a_i = \frac{1}{2\sqrt{Z_{0i}}} \left(V_i + Z_{0i} I_i \right), \tag{3.1}$$

where Z_{0i} is the characteristic impedance of i-th port and V_i and I_i are the voltage and current of i-th port. The reflected power waves also defined as

$$b_i = \frac{1}{2\sqrt{Z_{0i}}} \left(V_i - Z_{0i} I_i \right). \tag{3.2}$$

The input voltage and current are represented using a_i and b_i as

$$V_i = \sqrt{Z_{0i}} \left(a_i + b_i \right), I_i = \frac{1}{\sqrt{Z_{0i}}} \left(a_i - b_i \right). \tag{3.3}$$

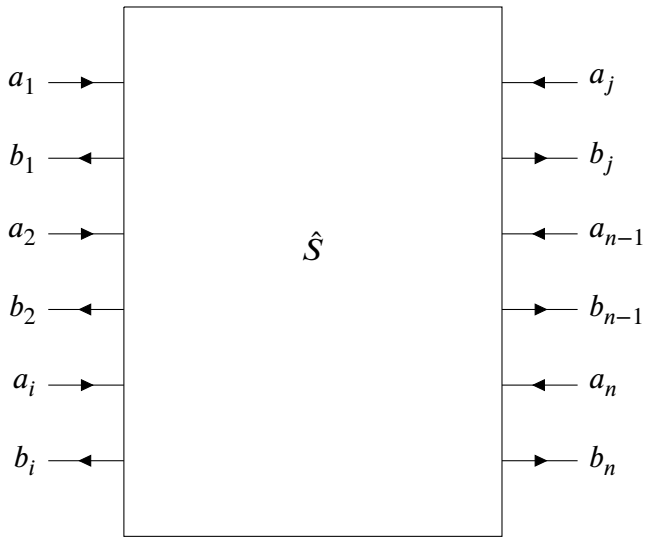


Fig. 3.1 N-port network and incident power waves and reflected power waves on the ports.

Matrix elements of the S-parameter are defined in relation to these incident and reflected power waves as

$$\vec{b} = \hat{S}\vec{a}, \tag{3.4}$$

where $\vec{a}$ and $\vec{b}$ are incident power wave vector and reflected power vector which are expressed as

$$\vec{a} = \begin{pmatrix} a_1 \\ a_2 \\ \vdots \\ a_i \\ \vdots \\ a_{n-1} \\ a_n \end{pmatrix} \tag{3.5}$$

and

$$\vec{b} = \begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_i \\ \vdots \\ b_{n-1} \\ b_n \end{pmatrix}, \tag{3.6}$$

respectively.

The matrix components of the S-parameter connected to N-port network are defined as follows:

$$S_{ii} = \left.\frac{b_i}{a_i}\right|_{\substack{a_k=0 \\ k=1,2,\ldots,N \\ k\neq i}}, \tag{3.7}$$

$$S_{ji} = \left.\frac{b_j}{a_i}\right|_{\substack{a_k=0 \\ k=1,2,\ldots,N \\ k\neq i}}. \tag{3.8}$$

If an impedance at a port i is defined as

$$Z_i = \frac{V_i}{I_i}, \tag{3.9}$$

a reflect coefficient Γ of the port i is written as

$$\Gamma_i = \frac{b_i}{a_i} \tag{3.10}$$

When a load of impedance Z_L is connected to the i-th port, the reflection coefficient Γ_i is written as

$$\Gamma_{\mathrm{i}} = \frac{Z_{\mathrm{L}} - Z_{0i}}{Z_{\mathrm{L}} + Z_{0i}}, \tag{3.11}$$

by substituting eq.(3.1) and (3.2) into eq. (3.10).

For example, the S-parameter of a two-port network can be written as

$$\begin{pmatrix} b_1 \\ b_2 \end{pmatrix} = \begin{pmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{pmatrix} \begin{pmatrix} a_1 \\ a_2 \end{pmatrix}, \tag{3.12}$$

$$S_{11} = \frac{b_1}{a_1}\Big|_{a_2=0}, S_{12} = \frac{b_1}{a_2}\Big|_{a_1=0}, \tag{3.13}$$

$$S_{21} = \frac{b_2}{a_1}\Big|_{a_2=0}, S_{22} = \frac{b_2}{a_2}\Big|_{a_1=0}. \tag{3.14}$$

In the calculation of the S-parameter, it is convenient to use the conversion between the S-parameter and other multi-terminal matrices such as Z, Y, and $ABCD$ matrices.

The Z matrix is defined as

$$\vec{V} = \hat{Z}\vec{I}, \tag{3.15}$$

where $\vec{V}$ is a vector representation of the voltage and $\vec{I}$ is the input current vector representation. $\vec{V}$ and $\vec{I}$ are defined as

$$\vec{V} = \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{pmatrix}, \tag{3.16}$$

$$\vec{I} = \begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{pmatrix}, \tag{3.17}$$

where I_i is the input current at i-th port and V_i is the voltage at i-th port. Similarly, Y matrix is defined as

$$\vec{I} = \hat{Y}\vec{V}. \tag{3.18}$$

Figure 3.2 shows the voltage and current definitions for a multiport network.

Then there are the following relations between the S-parameter and the Z and the Y matrices.

$$\hat{S} = \hat{Z_0}^{-1/2}(\hat{Z} - \hat{Z_0})(\hat{Z} + \hat{Z_0})^{-1}\hat{Z_0}^{1/2} \tag{3.19}$$

$$\hat{Z} = \hat{Z_0}^{1/2}(\hat{I} - \hat{S})^{-1}(\hat{I} + \hat{S})\hat{Z_0}^{1/2} \tag{3.20}$$

$$\hat{S} = \hat{Z_0}^{-1/2}(\hat{I} - \hat{Z_0}\hat{Y})(\hat{I} + \hat{Z_0}\hat{Y})^{-1}\hat{Z_0}^{1/2} \tag{3.21}$$

$$\hat{Y} = \hat{Z_0}^{-1/2}(\hat{I} + \hat{S})^{-1}(\hat{I} - \hat{S})\hat{Z_0}^{-1/2}. \tag{3.22}$$

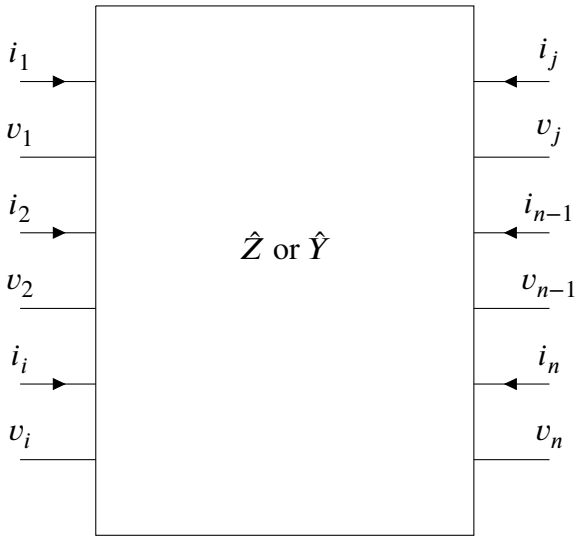


Fig. 3.2 Voltage and current definitions for a multiport network.

$$\hat{Z}_0 = diag(Z_i) \tag{3.23}$$

The $ABCD$ matrix is also useful for computing cascaded 2-terminal matrix elements. The ABCD matrix is defined as

$$\begin{pmatrix} v_1 \\ i_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_2 \\ i_2 \end{pmatrix}, \tag{3.24}$$

where v_i and i_i are defined as Fig. 3.3.

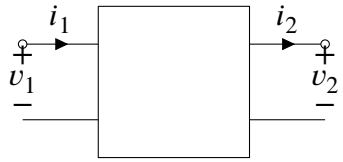


Fig. 3.3 ABCD matrix for two port network.

In the case of two ports, the conversion from Z matrix, Y matrix, and S-parameters to the $ABCD$ matrix can be written as follows:

$$\hat{F}_z = \begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} \dfrac{Z_{11}}{Z_{21}} & \dfrac{\Delta Z}{Z_{21}} \\ \dfrac{1}{Z_{21}} & \dfrac{Z_{22}}{Z_{21}} \end{pmatrix}, \tag{3.25}$$

where $\Delta Z = Z_{11}Z_{22} - Z_{12}Z_{21}$.

$$\hat{F}_y = \begin{pmatrix} -\dfrac{Y_{22}}{Y_{21}} & -\dfrac{1}{Y_{21}} \\ -\dfrac{\Delta Y}{Y_{21}} & -\dfrac{Y_{11}}{Y_{21}} \end{pmatrix}, \tag{3.26}$$

where $\Delta Y = Y_{11}Y_{22} - Y_{12}Y_{21}$.

$$\hat{F}_s = \begin{pmatrix} \dfrac{(1+S_{11})(1-S_{22}) + S_{12}S_{21}}{2S_{21}} & Z_0\dfrac{(1+S_{11})(1-S_{22}) - S_{12}S_{21}}{2S_{21}} \\ \dfrac{(1-S_{11})(1-S_{22}) - S_{12}S_{21}}{2S_{21}Z_0} & \dfrac{(1-S_{11})(1+S_{22}) + S_{12}S_{21}}{2S_{21}} \end{pmatrix}. \tag{3.27}$$

Conversely, the conversion from the $ABCD$ matrix to the Z matrix, the Y matrix and the S-parameter can be performed as follows.

$$\hat{Z} = \begin{pmatrix} \dfrac{A}{C} & \dfrac{\Delta ABCD}{C} \\ \dfrac{1}{C} & \dfrac{D}{C} \end{pmatrix}, \tag{3.28}$$

where $\Delta ABCD = AD - BC$.

$$\hat{Y} = \begin{pmatrix} \dfrac{D}{B} & -\dfrac{\Delta ABCD}{B} \\ -\dfrac{1}{B} & \dfrac{A}{B} \end{pmatrix}, \tag{3.29}$$

and

$$\hat{S} = \begin{pmatrix} \dfrac{A + B/Z_0 - CZ_0 - D}{\Psi} & \dfrac{2(AD - BC)}{\Psi} \\ \dfrac{2}{\Psi} & \dfrac{-A + B/Z_0 - CZ_0 + D}{\Psi} \end{pmatrix}, \tag{3.30}$$

where $\Psi = A + B/Z_0 + CZ_0 + D$.

For calculation of the S-parameter when a small-signal equivalent circuit is given, the ABCD matrix can be used to perform a simple matrix calculation eq. (A.2), (A.3) and (A.4) (Appendix A).

The S-parameter can be obtained directly from the defining equation, or it can be easily calculated by obtaining the matrix representation of the multi-terminal equivalent circuit model using the Z, Y, and ABCD matrices shown here, and then converting it to the S-parameter.

The S-parameter with cascade connections can be easily calculated using the chain scattering parameter, T matrix[75, 76].

For a general N-port S-parameter with cascade connections from m+1 to N, the T matrix can be written as

$$\begin{pmatrix} b_1 \\ b_2 \\ \vdots \\ b_m \\ a_1 \\ a_2 \\ \vdots \\ b_m \end{pmatrix} = \begin{pmatrix} T_{11} & T_{12} & \cdots & \cdots & T_{1N} \\ T_{21} & T_{22} & \cdots & \cdots & T_{2N} \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ \vdots & \vdots & \vdots & \cdots & \vdots \\ T_{M1} & T_{M2} & \cdots & \cdots & T_{MN} \end{pmatrix} \begin{pmatrix} a_{m+1} \\ a_{m+2} \\ \vdots \\ a_{m+n} \\ b_{m+1} \\ b_{m+2} \\ \vdots \\ b_{m+n} \end{pmatrix}. \tag{3.31}$$

Although there are some definition of T matrix, the definition shown in eq. (3.31) is used in this study.

For a four port network, T-matrix and S-matrix can be decomposed into 2 x 2 partial matrix as follow:

$$\begin{pmatrix} T_{11} & T_{12} & T_{13} & T_{14} \\ T_{21} & T_{22} & T_{23} & T_{24} \\ T_{31} & T_{32} & T_{33} & T_{34} \\ T_{41} & T_{42} & T_{43} & T_{44} \end{pmatrix} = \begin{pmatrix} \hat{T}_{I,I} & \hat{T}_{I,II} \\ \hat{T}_{II,I} & \hat{T}_{II,II} \end{pmatrix} \tag{3.32}$$

and

$$\begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} \\ S_{21} & S_{22} & S_{23} & S_{24} \\ S_{31} & S_{32} & S_{33} & S_{34} \\ S_{41} & S_{42} & S_{43} & S_{44} \end{pmatrix} = \begin{pmatrix} \hat{S}_{I,I} & \hat{S}_{I,II} \\ \hat{S}_{II,I} & \hat{S}_{II,II} \end{pmatrix}. \tag{3.33}$$

Then S-matrix and T-matrix are written as

$$\begin{pmatrix} \hat{S}_{I,I} & \hat{S}_{I,II} \\ \hat{S}_{II,I} & \hat{S}_{II,II} \end{pmatrix} = \begin{pmatrix} \hat{T}_{I,II}\hat{T}_{II,II}^{-1} & \hat{T}_{I,I} - \hat{T}_{I,II}\hat{T}_{II,II}^{-1}\hat{T}_{II,I} \\ \hat{T}_{II,II}^{-1} & -\hat{T}_{II,II}^{-1}\hat{T}_{II,I} \end{pmatrix} \tag{3.34}$$

and

$$\begin{pmatrix} \hat{T}_{I,I} & \hat{T}_{I,II} \\ \hat{T}_{II,I} & \hat{T}_{II,II} \end{pmatrix} = \begin{pmatrix} \hat{S}_{I,II} - \hat{S}_{I,I}\hat{S}_{II,I}^{-1}\hat{S}_{II,II} & \hat{S}_{I,I}\hat{S}_{II,I}^{-1} \\ -\hat{S}_{II,I}^{-1}\hat{S}_{II,II} & \hat{S}_{II,I}^{-1} \end{pmatrix}. \tag{3.35}$$

The conversion formulas from a scattering matrix to a transfer scattering matrix $\hat{T}$ of a 2-ports network is written as

$$\hat{T} = \frac{1}{S_{21}} \begin{pmatrix} S_{12}S_{21} - S_{11}S_{22} & S_{11} \\ -S_{22} & 1 \end{pmatrix}. \tag{3.36}$$

3.2 Signal flow graph

One of the methods to describe RF networks is a signal flow graph. In this section, a general theory of signal flow graphs is described.

In a signal flow graph, the matrix elements of the S-parameter are represented as transitions between nodes corresponding to power waves. For example, the equation of a reflected wave b for an incident wave a

$$b = \Gamma a \tag{3.37}$$

is written in a signal flow graph as shown in Fig. 3.4(a).

When nodes are connected in series, the signal flow graph can transform as shown in Fig. 3.4(b). This corresponds to transforming

$$b = S_{ba}a, \tag{3.38}$$

$$c = S_{cb}b \tag{3.39}$$

into

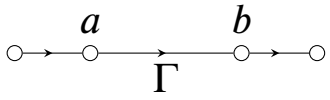
$$c = S_{cb}S_{ba}a. \tag{3.40}$$

In the case of a parallel connection, it can be transformed as 3.4(c), This relation corresponds to

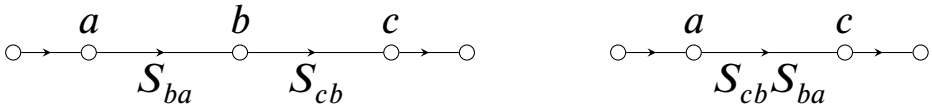
$$b = S_{b_1a}a + S_{b_2a}a = \left(S_{b_1a} + S_{b_2a}\right)a. \tag{3.41}$$

Splitting the branch can be transformed the signal flow graph as 3.4(d). This transform corresponds to

$$d = S_{dc}\left(S_{ca}a + S_{cb}b\right) = S_{dc}S_{ca}a + S_{dc}S_{cb}b. \tag{3.42}$$



(a) Description of nodes and power waves in signal flow graph



(b) Series connection in signal flow graph

(c) Parallel connection of signal flow graph

(d) Splitting of branches.

(e) Self loop

Fig. 3.4 Description of the signal flow graph.

When there is a loop, the signal flow graph can be transformed as 3.4(e). This corresponds to transforming

$$b = a + \Gamma b, \tag{3.43}$$

$$c = b \tag{3.44}$$

into

$$c = \frac{1}{1-\Gamma}a. \tag{3.45}$$

The signal gain can be calculated from the signal flow graph using these rules. As a simple example, the S-parameter of a single device can be calculated in the following step.

An S-paraemeter of a FET S is connected to Γ_S and Γ_L as shown in Fig. 3.5. The right side loop looking from port 1 is define as Γ_{in}.

Γ_{in} can be calculated using a signal flow graph as Fig.3.6. Then, the loop gain from a_1 to b_1 is written as

$$\frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}. \tag{3.46}$$

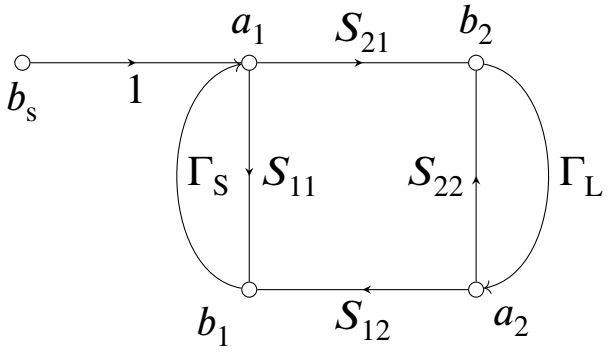


Fig. 3.5 Signal flow graph for two port network.

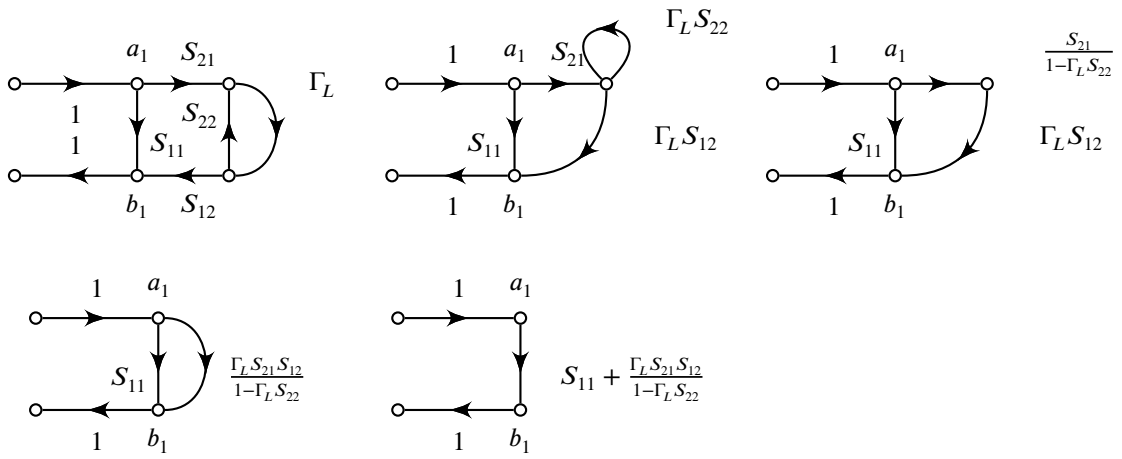


Fig. 3.6 Transformation of the signal flow graph

A particular loop gain of a circuit consist of parallel connected devices can be calculated using signal flow graph or the S-parameter calculated with matrix calculation. In the latter method, an S-parameter of parallel connected devices can be calculated using Z matrix, Y matrix and ABCD matrix.

In this section, the signal flow graph method will be discussed. Figure 3.7 shows the FETs connected in parallel to a source and a load.

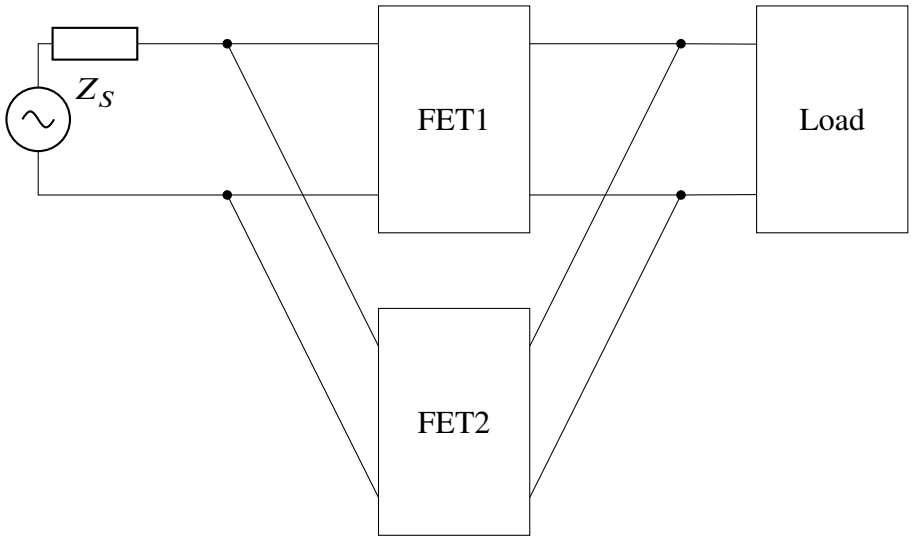


Fig. 3.7 Sourced and loaded FETs connected in parallel

It is assumed that the input signal from the gate is input to FET_1 and FET_2. Here, the impedance of the path is assumed to be zero, and the case of ideal wiring is considered.

These three ports tee can be written as

$$S = \frac{1}{3}\begin{pmatrix} -1 & 2 & 2 \\ 2 & -1 & 2 \\ 2 & 2 & -1 \end{pmatrix} \tag{3.47}$$

using the definition of the S-parameter.

The Signal flow graph for this is shown in Fig. 3.8. Similarly, if the drain terminal is also connected with the 3 ports connected tee, the parallel connection of two devices can be written as Fig. 3.9 using the signal flow graph of S-parameter.

Mason's rule [77] is used to calculate the loop gain of a circuit. Mason's rule provides a method to compute the path of the transfer function without any omissions.

First, follow the steps below to find the forward path and loop.

- step 1: Find the forward path. Find a path that connects one node to another node toward the branch that connects the two nodes and does not pass through the same node twice. The gains of the found paths are denoted as $P_1, P_2, ..., P_n$ respectively. P denotes the set of these paths.

- step 2: Find the Loop. Find a loop path that branches from a node in the path described above, connects to a node behind it, and does not pass through the same node twice. Let the gain of this path be $L_1, L_2, ..., L_m$. Let $L_1, L_2, ..., L_m$ be the gains of this path,

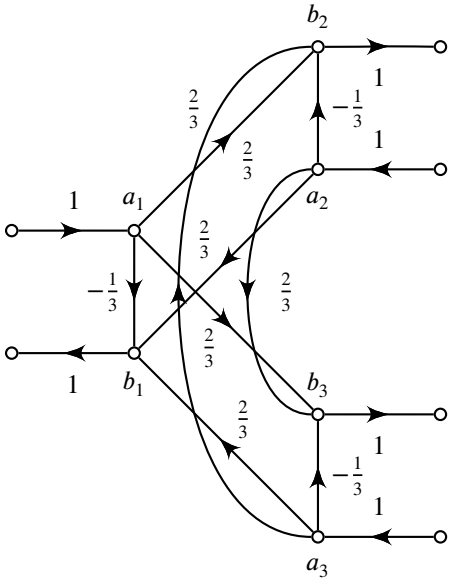


Fig. 3.8 The signal flow graph on the 3 ports connection.

and denote the set by $L(1)$. Also, let $L(1)^i$ be the set of loops of the first order that do not touch the forward path P_i.

- step 3: Find the combination of two independent loops that do not share a node with each other, and take the product of each combination. Let $L(2)$ be the set of these quadratic loop combinations and $\sum L(2)^k$ be the quadratic loop combination that does not touch the path P_k.

- step 4: Find three independent combinations of loops that do not share a node with each other, and take the product of each combination. Let $L(3)$ be the set of loop combinations. Let $\sum L(3)^k$ denote the combination of cubic loops unconnected to the path P_k. In the same way, the combinations of loops are obtained up to higher order (m).

Mason's rule can be used to obtain the transfer function using the results as follows.

$$\frac{b}{a} = \frac{1}{\Delta}\sum_{i=1}^{P} P_i \delta_i, \tag{3.48}$$

where Δ is given as

$$\Delta = \quad 1 - \sum L(1) + \sum L(2)... + (-1)^m L(m)..., \tag{3.49}$$

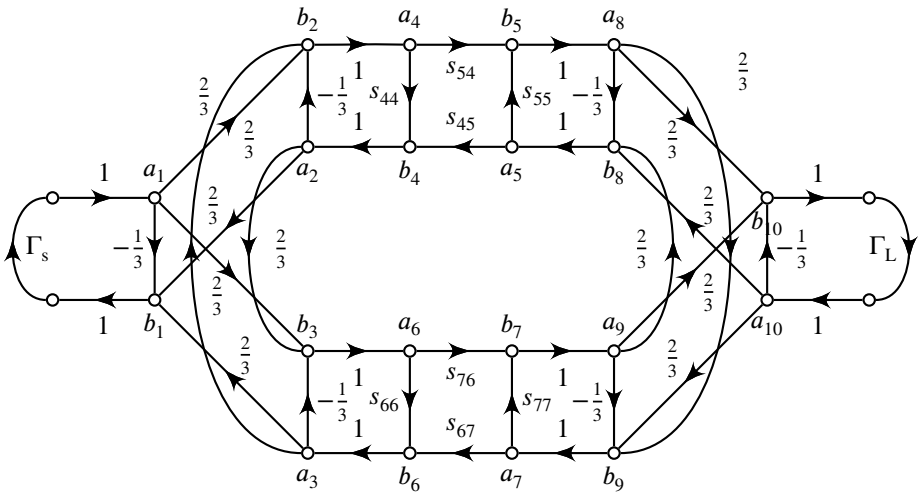


Fig. 3.9 The signal flow graph of the circuit composed parallel connected devices.

and δ_k is given as

$$\delta_k = 1 - \sum L(1)^k + \sum L(2)^k ... + (-1)^m \sum L(m)^k + ... \tag{3.50}$$

3.3 Novel stability analysis criteria for integrated design in power electronics circuits

This study proposes a method for system optimization that incorporates the internal state of the device. The computation time cost for transient simulation in TCAD is too large to carry out device and circuit parameters optimization. Additionally, the simulation does not always converge when the circuit system is unstable. To solve these problems, a novel analysis method using S-parameters calculated by TCAD simulation and signal flow graphs is proposed in this study.

Fig. 3.10 presents the concept of the proposed method. The device parameters of the switching devices such as IGBTs or MOSFETs, are calculated by TCAD simulation. The module and circuit parameters are measured experimentally or calculated by either analytical calculation or electro-magnetic simulation. S-parameters are derived from the device and the circuit parameters. The oscillation conditions are calculated using signal flow analysis and a Nyquist diagram with the S-parameter. These results are fed back to the device, package, and circuit design. This method can reduce the calculation time required for circuit parameter optimization.

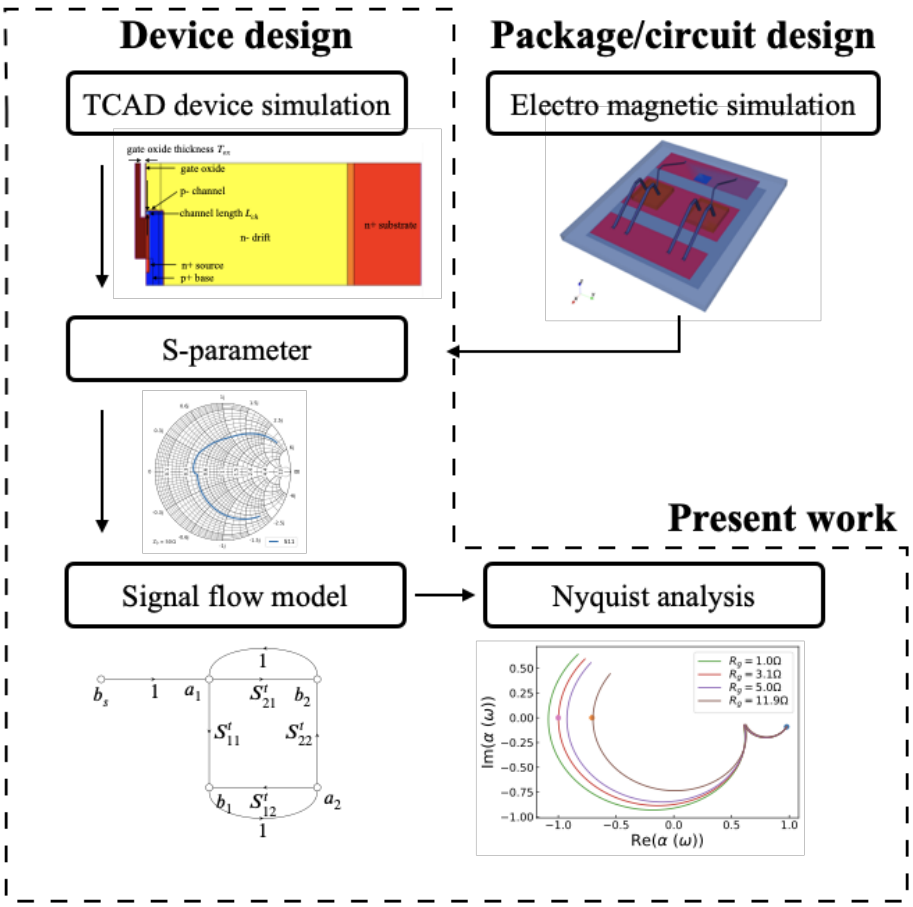


Fig. 3.10 The proposed concept of design flow integrates device, package and circuit design.

In this model, the S-parameter calculated by the TCAD simulation at the assumed operating point is used instead of the SPICE model calculated from the TCAD simulation results which is commonly used in previous studies. This has the advantage that changes in the internal state of the device can be directly incorporated into the stability analysis and the relationship between the stability analysis results and the internal state of the device can be directly investigated.

For stability analysis, Nyquist plots are used based on the loop gain from the signal flow graph. In this way, not only the circuit and device conditions for suppressing oscillation can be obtained, but also the conditions for suppressing oscillation with a particular phase and gain margin can be calculated. Since ensuring operating stability is generally a trade-off with characteristics, an evaluation method that can quantitatively set an appropriate margin is effective in optimizing the design of power systems.

In the proposed method, the analysis is carried out in the following steps.

- Determining the operating point to be analyzed

- Deriving the equivalent circuit at the operating point
- Determining the S-parameter of the power device using TCAD simulation.
- Calculating the loop gain using the signal flow graph
- Estimating oscillation conditions using Nyquist plot

In the following, these procedures will be explained by applying them to the analysis of the oscillation phenomenon that occurs during the type II short circuit.

Step 1: Determining the operating point to be analyzed

The first step is determining the circuit operating point to be analyzed. For example, the transient state of the switching operation of MOSFETs or IGBTs in the normal operating condition of the system, the state in which a large current surge is input, the state in which external noise is input, and so on, are selected as the circuit operating states to be considered in the system design. In this study, although the analysis is focused on the short-circuit operation mode of Type II, the method itself can be used in general for power system design. In particular, unlike SPICE simulation and TCAD transient analysis, the advantage of this method is that it can directly calculate the stability of arbitrary states and quantitatively estimate the margin of the stability of those states.

To consider the short circuit mode of Type II, the circuit shown in Fig. 3.11 is considered. When the MOSFET on the low side is completely on and a constant current flows, the high side is turned on to create a short circuit state.

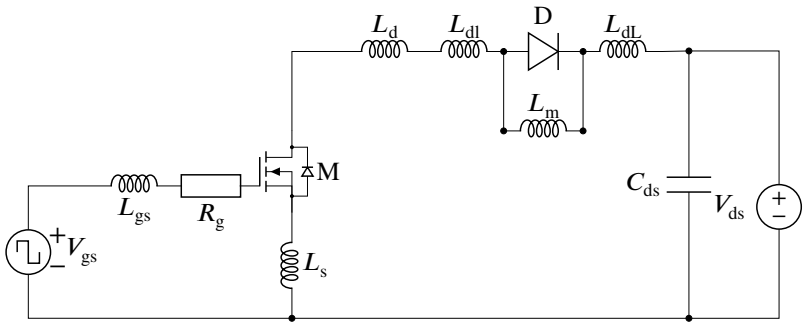


Fig. 3.11 Chopper circuit investigated in this paper. The circuit consists of a high-side diode and a low-side MOSFET.

Step 2: Deriving an equivalent circuit

The next step is to derive the equivalent circuit for the operating point selected at step 1. Since the short-circuit condition of the load is considered, the diode D on the high side and L_{m} are replaced by a short circuit. The capacitance of the power supply and the capacitance connected in parallel with the power supply are also assumed to be sufficiently large and are replaced by shorts. Then the chopper circuit presented in Fig. 3.11 can be transformed to the equivalent small-signal circuit shown in Fig. 3.12. In this equivalent ciruite, Z_{L} is defined as $Z_{\mathrm{L}} = j\omega L_{\mathrm{dL}}$.

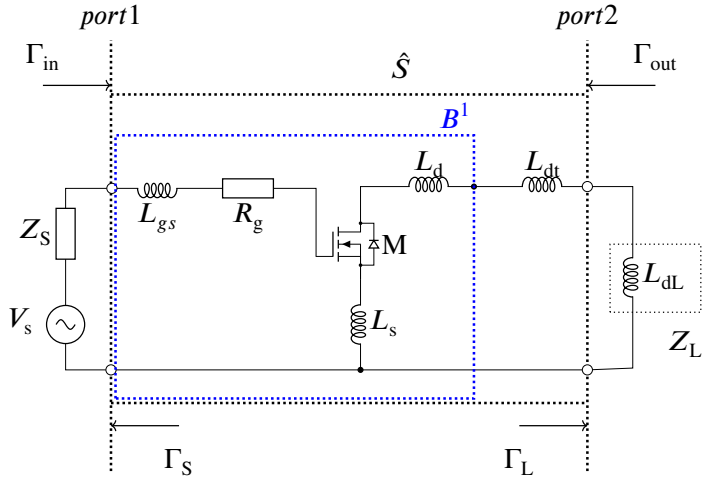


Fig. 3.12 Simplified equivalent circuit.

Step 3: Calculating an S-parameter for a power device using TCAD simulation

In the next step, the S-parameters of the power device are calculated using TCAD simulation.

S-parameters under specific operating conditions can be calculated using the small-signal AC analysis function of the TCAD simulator [78]. The AC analysis computes the admittance matrix $\hat{Y}$ between circuit nodes. When the voltage variant of node j is δV for the current variant δI of node k, $\hat{Y}$ can be written as

$$\delta I_j = Y_{jk}\delta V_k. \tag{3.51}$$

The Y-matrix can be transformed to the S-parameter matrix as

$$\hat{S} = (\hat{E} - Z_0\hat{Y}) \cdot (\hat{E} + Z_0\hat{Y})^{-1}, \tag{3.52}$$

where Z_0 and $\hat{E}$ are the specific impedance and the unit matrix, respectively.

Step 4: Calculating oscillation condition factor from the signal flow graph

The next step is calculating the oscillation condition factor from the signal flow graph to analyze the stability of the circuit operation.

First, a signal flow graph is created using the equivalent circuit calculated in step 2 and the S-parameter calculated in step 3.

Next, the loop gain of the device to be focused on is calculated using Mason's rule.

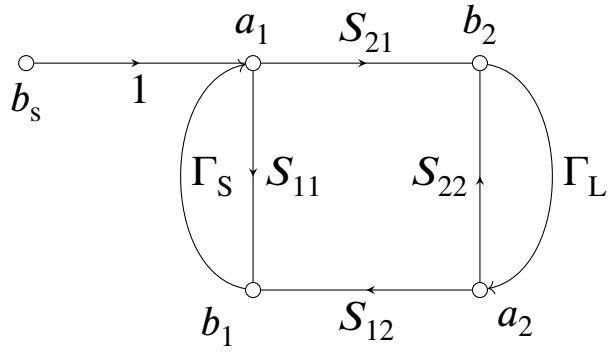


Fig. 3.13 Equivalent Signal flow graph.

There are two ways to create a signal flow graph: one is to connect the S-parameters of individual components in the signal flow graph, and the other is to connect the components by matrix calculation and then convert it to S-parameters. The details are explained in the next section. In this section, the latter method is used to calculate the oscillation conditions.

The signal flow graph can be written as shown in the Fig. 3.13, where $\hat{S}$ is the S-parameter with integrated circuit elements. The input and reflection at port 1 can be written as follows, respectively.

$$a_1 = b_s + \Gamma_S b_1, \tag{3.53}$$

$$b_1 = \Gamma_{in} a_1. \tag{3.54}$$

By substituting 3.53 into 3.54,

$$b_1(1 - \Gamma_S \Gamma_{in}) = b_s \Gamma_{in}. \tag{3.55}$$

Hence, loop gain is written as

$$\frac{b_1}{b_s} = \frac{\Gamma_{in}}{(1-\Gamma_S\Gamma_{in})}. \tag{3.56}$$

The oscillation condition can be considered as the denominator of eq. (3.56) is zero at a particular frequency.

$$1-\Gamma_S\Gamma_{in} = 1-\left(S_{11}+\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right)\Gamma_S = 0. \tag{3.57}$$

The Nyquist stability condition is used to compute the oscillation condition. The oscillation condition factor is defined as

$$\alpha(\omega) = -\left(S_{11}+\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right)\Gamma_S\cdot, \tag{3.58}$$

in this study.

Step 5: Estimating the oscillation conditions using Nyquist plot

The next step is to estimate the oscillation conditions using a Nyquist plot for stability analysis.

The S_{11}, S_{12}, S_{21} and S_{22} in the equation (3.58) are complex numbers depending on ω. To evaluate the oscillation condition factor, $\alpha(\omega)$ is plotted on a complex plane for each ω as Nyquist plot. The circuit becomes unstable when a locus passes to the left of the (-1,0) point. When the locus passes on the (-1,0), the circuit is under the critical condition. When the locus is located to the right of (-1,0), the circuit becomes stable and the distance from (-1,0) to the locus can be regarded as the margin. Therefore, quantitative stabilization can be performed. These relationships are shown in Fig. 3.14.

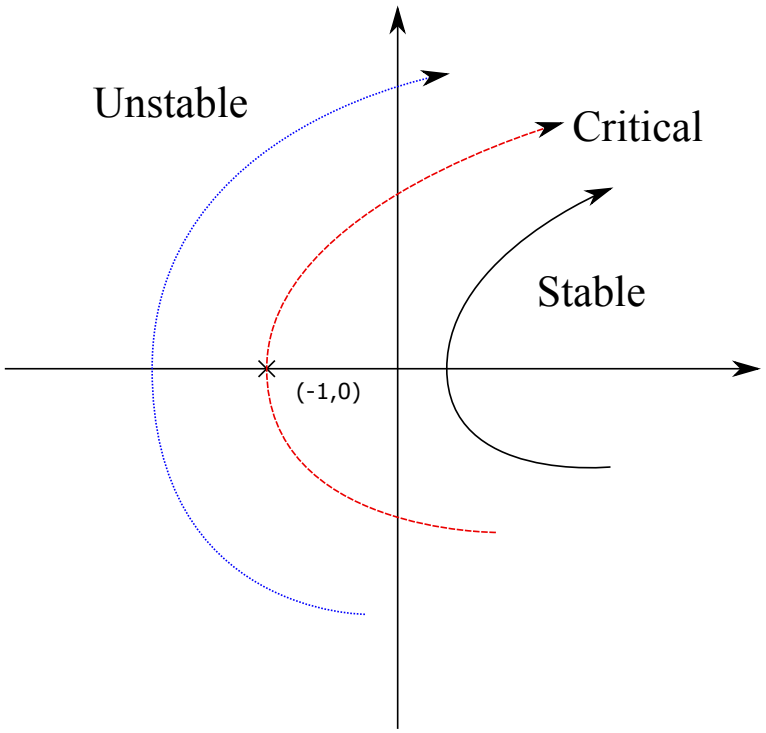


Fig. 3.14 Nyquist plot of the oscillation condition factor.

3.4 Oscillation condition factor for parallel connected power switches

In this section, oscillation in a circuit in which MOSFETs are connected in parallel is considered. Because MOSFETs are generally connected in parallel in high-power modules, it is important to determine the circuit parameter for the stable operation of MOSFETs connected in parallel. Feedback signal loops via parallel-connected MOSFETs can decrease the stability of the circuit compared to a circuit consisting of a single MOSFET as described in the previous section.

The stability analysis method for parallel connection will be discussed using a chopper circuit, as shown in Fig. 3.15 and 3.16(a).

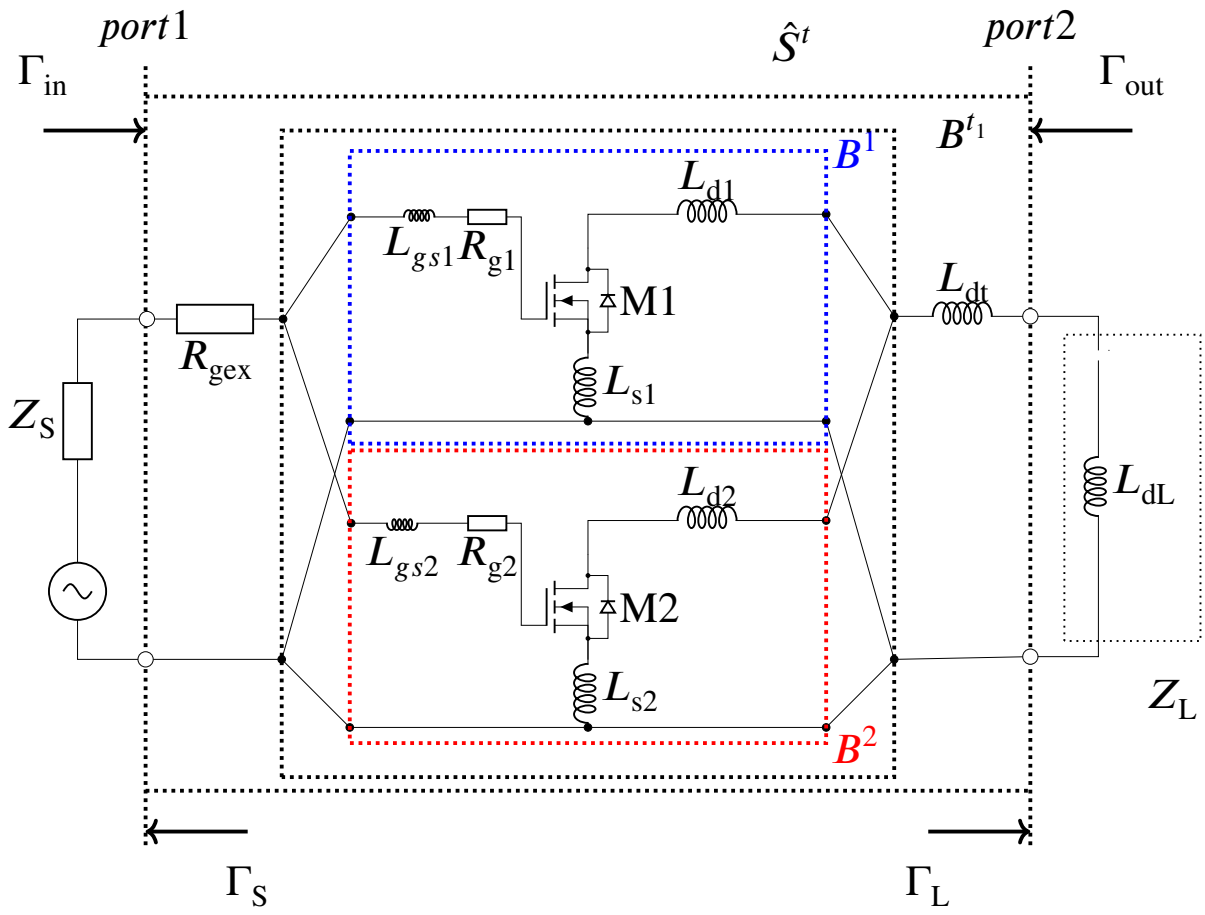


Fig. 3.15 Simplified small signal equivalent circuit

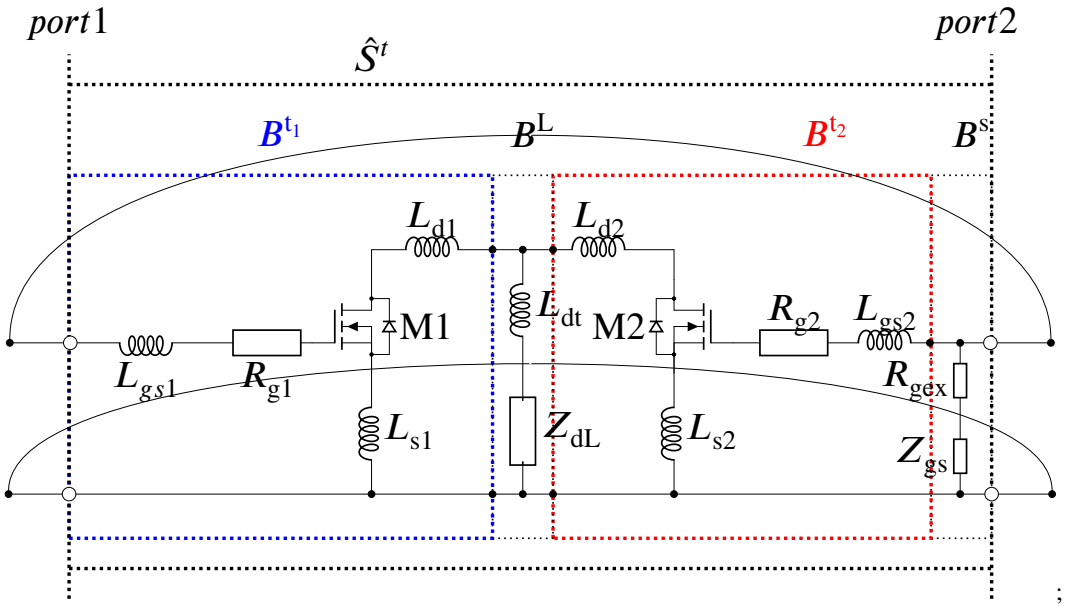
The oscillation condition factor $\alpha(\omega)$ can apply to a multi-chip case. The oscillation condition factor $\alpha(\omega)$ can be written as

$$\alpha(\omega) = -\left(S^t_{11} + \frac{S^t_{12}S^t_{21}\Gamma_L}{1 - S^t_{22}\Gamma_L}\right)\Gamma_S, \tag{3.59}$$

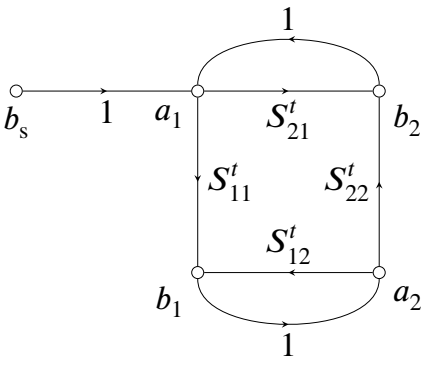
where Γ_S and Γ_L are the input and the load reflection coefficient, respectively.

However, the oscillation condition factor $\alpha(\omega)$ can only compute the common oscillation mode. When MOSFETs are symmetrically connected and with low impedance, the oscillation can be induced by differential oscillation mode [49, 48]. To compute this mode, the other signal flow diagram is introduced. Figure 3.16(a) and 3.16(b) show the equivalent circuit and the signal flow graph of this oscillation mode. In this equivalent circuit, the input signal is transferred through the drain of MOSFETs to the gate of the second MOSFET. After the signal passes through the gate of the second MOSFET, the signal is fed back to the gate signal of the first MOSFET.

To compute the stability of the circuit, a virtual ground and virtual signal source at port 1, shown in Fig. 3.16(a) are assumed. b_s is the virtual input signal. a_1, b_1, a_2, and b_2 are power waves. $\hat{S}^t$ is an S-parameter of two-port network consisting of power MOSFETs and passive components as shown in Fig. 3.16(a). $\hat{S}^t$ can be computed from the TCAD simulation results of the MOSFET using the signal flow-graph analysis technique.



(a) Simplified small signal equivalent circuit



(b) Signal flow graph

Fig. 3.16 Simplified equivalent circuit and signal flow graph to evaluate the oscillation condition.

According to the signal flow graph shown in Fig. 3.16(b), signal flow b_2 to a_1 is written as

$$a_1 = b_s + b_2. \tag{3.60}$$

Alternatively, signal flow a_1 to b_2 is written as

$$b_2 = \left(S_{21}^t + \frac{S_{11}^t S_{22}^t}{1 - S_{12}^t} \right) a_1 = \Gamma_{\text{in}} a_1. \tag{3.61}$$

By inserting eq. (3.60) into eq. (3.61), we obtain

$$b_2(1 - \Gamma_{\text{in}}) = b_{\text{s}} \Gamma_{\text{in}}. \tag{3.62}$$

Loop gain is written as

$$\frac{b_1}{b_{\text{s}}} = \frac{\Gamma_{\text{in}}}{(1 - \Gamma_{\text{in}})}. \tag{3.63}$$

The oscillation condition can be written as

$$1 - \Gamma_{\text{in}} = 1 - \left(S_{21}^t + \frac{S_{11}^t S_{22}^t}{1 - S_{12}^t} \right) = 0., \tag{3.64}$$

For the Nyquist plot, the new other oscillation condition factor

$$\beta(\omega) = - \left(S_{21}^t + \frac{S_{11}^t S_{22}^t}{1 - S_{12}^t} \right). \tag{3.65}$$

is defined.

3.5 S-parameter calculation for power switches connected with circuit components

In this section, details of a calculation procedure are discussed. First, the loop gain of the circuit consisting of a single MOSFET is considered. Second, the loop gain of the circuit consisting of MOSFETs connected in parallel is discussed.

3.5.1 S-parameter for single power switch

The equivalent circuit shown in Fig. 3.12 is considered here. The admittance matrix of the MOSFET $\hat{Y}^M$ is given by eq.(3.51).

The impedances of the parasitic elements of the MOSFET in Fig. 3.12 are written as

$$Z_{\mathrm{s}} = j\omega L_{\mathrm{s}}, \tag{3.66}$$

$$Z_{\mathrm{d}} = j\omega L_{\mathrm{d}}, \tag{3.67}$$

$$Z_{\mathrm{g}} = R_{\mathrm{g}} + j\omega L_{\mathrm{gs}}. \tag{3.68}$$

The admittance matrix $\hat{Y}^t$ attached to parasitic inductance and gate resistance can be obtained as follows:

$$\hat{Y}^M = \frac{1}{\gamma}\begin{pmatrix} Y_{11}^t + \Delta Y^t(Z_{\mathrm{s}} + Z_{\mathrm{d}}) & Y_{12}^t - \Delta Y^t Z_{\mathrm{s}} \\ Y_{21}^t - \Delta Y^t Z_{\mathrm{s}} & Y_{22}^t + \Delta Y^t(Z_{\mathrm{s}} + Z_{\mathrm{g}}) \end{pmatrix}, \tag{3.69}$$

where

$$\Delta Y^t = Y_{11}^t Y_{22}^t - Y_{12}^t Y_{21}^t, \tag{3.70}$$

$$\begin{aligned} \gamma = {} & 1 + (Y_{11}^t + Y_{12}^t + Y_{21}^t + Y_{22}^t)Z_{\mathrm{s}} \\ & + Y_{11}^t Z_{\mathrm{gs}} + Y_{22}^t Z_{\mathrm{d}} \\ & + \Delta Y^t(Z_{\mathrm{d}} Z_{\mathrm{gs}} + Z_{\mathrm{gs}} Z_{\mathrm{s}} + Z_{\mathrm{s}} Z_{\mathrm{d}}). \end{aligned} \tag{3.71}$$

Using Y-matrix, S-parameter matrix can be written as

$$\hat{S}^t = (\hat{E} - Z_0 \hat{Y}^t) \cdot (\hat{E} + Z_o \hat{Y}^t)^{-1}, \tag{3.72}$$

where Z_0 and $\hat{E}$ are the specific resistance and the unit matrix, respectively.

3.5.2 S-parameter for power switches connected in parallel

In this section, oscillation in a circuit in which MOSFETs are connected in parallel, as shown in Fig. 3.15 is considered. To calculate the oscillation condition factor $\alpha(\omega)$ and $\beta(\omega)$, it is necessary to calculate the S-parameters $\hat{S}^t$ for each of $\alpha(\omega)$ and $\beta(\omega)$.

By introducing a network block B^{t_1} including n blocks of B^i connected parallelly as shown in Fig. 3.15, the S-parameter of a multi-chip circuit $\hat{S}^t$ for $\alpha(\omega)$ can be computed from the TCAD simulation results of the MOSFET as following.

A network block B^n consists of FET and parasitic components, as shown in Fig. 3.15 and 3.16(a).

The impedances of the parasitic elements of the MOSFET are written as

$$Z_{si} = j\omega L_{si}, \tag{3.73}$$

$$Z_{di} = j\omega L_{di}, \tag{3.74}$$

$$Z_{gi} = R_{gi} + j\omega L_{gsi}. \tag{3.75}$$

Therefore, the admittance matrix $\hat{Y}^i$ of i-th MOSFET the attached parasitic inductances and the gate resistance can be obtained as follows:

$$\hat{Y}^i = \frac{1}{\gamma}\begin{pmatrix} Y_{11}^{M_i} + \Delta Y^{M_i}(Z_{si} + Z_{di}) & Y_{12}^{M_i} - \Delta Y^{M_i} Z_{si} \\ Y_{21}^{M_i} - \Delta Y^{M_i} Z_{si} & Y_{22}^{M_i} + \Delta Y^{M_i}(Z_{si} + Z_{gi}) \end{pmatrix}, \tag{3.76}$$

where

$$\Delta Y^{M_i} = Y_{11}^{M_i} Y_{22}^{M_i} - Y_{12}^{M_i} Y_{21}^{M_i}, \tag{3.77}$$

$$\begin{aligned} \gamma = {} & 1 + (Y_{11}^{M_i} + Y_{12}^{M_i} + Y_{21}^{M_i} + Y_{22}^{M_i}) Z_{si} \\ & + Y_{11}^{M_i} Z_{gsi} + Y_{22}^{M_i} Z_{di} \\ & + \Delta Y^{M_i}(Z_{di} Z_{gsi} + Z_{gsi} Z_{si} + Z_{si} Z_{di}). \end{aligned} \tag{3.78}$$

The Y-matrix of the network block B^{t_j} can be calculated from the sum of the Y^i. This is written as

$$\hat{Y}^{\mathrm{t_j}} = \sum_i^n \hat{Y}^i. \tag{3.79}$$

Using this Y-matrix, S-parameter matrix $\hat{S}^{t_j}$ can be written as

$$\hat{S}^{t_j} = (\hat{E} - Z_0 \hat{Y}^{t_j}) \cdot (\hat{E} + Z_o \hat{Y}^{t_j})^{-1}, \tag{3.80}$$

where Z_0 and $\hat{E}$ are the specific resistance and the unit matrix, respectively.

$\alpha(\omega)$

In calculating $\hat{S}^t$ for $\alpha(\omega)$, other parasitic components need to be considered. The conversion formula from a scattering matrix to a transfer scattering matrix $\hat{T}$ is written as

$$\hat{T}^{\mathrm{t_1}} = \frac{1}{S_{21}^{t_1}} \begin{pmatrix} S_{12}^{t_1} S_{21}^{t_1} - S_{11}^{t_1} S_{22}^{t_1} & S_{11}^{t_1} \\ -S_{22}^{t_1} & 1 \end{pmatrix}. \tag{3.81}$$

For simplicity, the impedances of the parasitic element are written as

$$Z_{\mathrm{dt}} = j\omega L_{\mathrm{dt}}, \tag{3.82}$$

$$Z_{\mathrm{gex}} = R_{\mathrm{gex}}. \tag{3.83}$$

The transfer scattering matrices are written as

$$\hat{T}^{\mathrm{s}} = \frac{1}{2Z_0} \begin{pmatrix} 2Z_0 - Z_{\mathrm{gex}} & Z_{\mathrm{gex}} \\ -Z_{\mathrm{gex}} & 2Z_0 + Z_{\mathrm{gex}} \end{pmatrix} \tag{3.84}$$

and

$$\hat{T}^{\mathrm{L}} = \frac{1}{2Z_0} \begin{pmatrix} 2Z_0 - Z_{\mathrm{dt}} & Z_{\mathrm{dt}} \\ -Z_{\mathrm{dt}} & 2Z_0 + Z_{\mathrm{dt}} \end{pmatrix}. \tag{3.85}$$

The net transfer scattering matrix can be derived from the product of these matrix as follow,

$$\hat{T}^h = \hat{T}^s \cdot \hat{T}^{t_1} \cdot \hat{T}^L. \tag{3.86}$$

Now, the total scattering matrix can be calculated as

$$\hat{S}^{\mathrm{t}} = \frac{1}{T_{22}^h} \begin{pmatrix} T_{12}^h & T_{11}^h T_{22}^h - T_{12}^h T_{21}^h \\ 1 & -T_{21}^h \end{pmatrix}. \tag{3.87}$$

$\beta(\omega)$

For the oscillation condition factor $\beta(\omega)$ when $n = l + k$ MOSFETs connected parallelly, a network block B^{t_1} including l blocks of B^i connected parallelly are considered. The S-matrix of $\hat{B}^{\mathrm{t_1}}$ can be calculated from eq. (3.80).

The conversion formula from a scattering matrix to a transfer scattering matrix $\hat{T}^{t_1}$ is written as

$$\hat{T}^{\mathrm{t}_1} = \frac{1}{S_{21}^{t_1}} \begin{pmatrix} S_{12}^{t_1} S_{21}^{t_1} - S_{11}^{t_1} S_{22}^{t_1} & S_{11}^{t_1} \\ -S_{22}^{t_1} & 1 \end{pmatrix}. \tag{3.88}$$

Similarly, by using a network block B^{t_2} including n blocks of B^j connected parallelly, the S-matrix $\hat{S}^{\mathrm{t}_2}$ can be calculated from eq. (3.80). The conversion formula from a scattering matrix to a transfer scattering matrix $\hat{T}^{t_2}$ is written as

$$\hat{T}^{\mathrm{t}_2} = \frac{1}{S_{12}^{t_2}} \begin{pmatrix} S_{12}^{t_2} S_{21}^{t_2} - S_{11}^{t_2} S_{22}^{t_2} & S_{11}^{t_2} \\ -S_{22}^{t_2} & 1 \end{pmatrix}. \tag{3.89}$$

For simplicity, the impedances of the parasitic element are rewritten as

$$Z_{\mathrm{dLt}} = Z_{\mathrm{dL}} + j\omega L_{\mathrm{dt}}, \tag{3.90}$$

$$Z_{\mathrm{gex}} = R_{\mathrm{gex}} + Z_{\mathrm{gs}}. \tag{3.91}$$

The transfer scattering matrices are written as

$$\hat{T}^{\mathrm{s}} = \frac{1}{2Z_{gex}} \begin{pmatrix} 2Z_{\mathrm{gex}} - Z_0 & -Z_0 \\ Z_0 & 2Z_{\mathrm{gex}} + Z_0 \end{pmatrix} \tag{3.92}$$

and

$$\hat{T}^{\mathrm{L}} = \frac{1}{2Z_{dLt}} \begin{pmatrix} 2Z_{\mathrm{dLt}} - Z_0 & -Z_0 \\ Z_0 & 2Z_{\mathrm{dLt}} + Z_0 \end{pmatrix}. \tag{3.93}$$

The net transfer scattering matrix can be derived from the product of these matrices as follow,

$$\hat{T}^h = \hat{T}^{t_1} \cdot \hat{T}^L \cdot \hat{T}^{t_2} \cdot \hat{T}^s. \tag{3.94}$$

Now, the total scattering matrix can be calculated as

$$\hat{S}^{\mathrm{t}} = \frac{1}{T_{22}^h} \begin{pmatrix} T_{12}^h & T_{11}^h T_{22}^h - T_{12}^h T_{21}^h \\ 1 & -T_{21}^h \end{pmatrix}. \tag{3.95}$$

3.6 Comparison of oscillation conditions determined from S-parameter and transfer function

In this section, the correspondence between the oscillation condition calculated using S-parameter and that determined using the transfer function will be confirmed.

The oscillation condition of a Colpitts oscillator is discussed as an example circuit for which an analytical solution of the oscillation condition can be easily obtained.

A circuit diagram of the Colpitts transmitter is shown in Fig. 3.17. Figure 3.18 shows a small-signal model for a MOSFET.

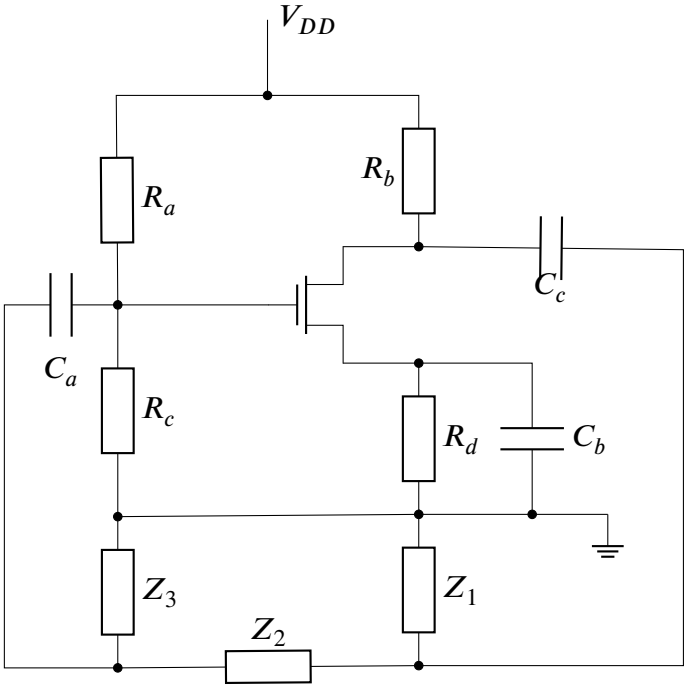


Fig. 3.17 Circuit of Colpitts oscillator.

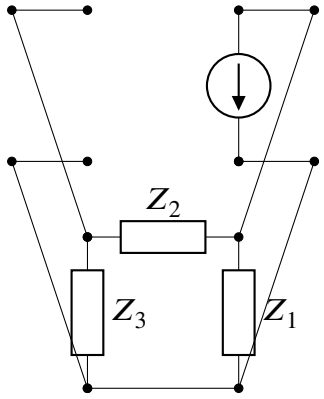


Fig. 3.18 Small signal equivalent circuit for the Colpitts oscillator.

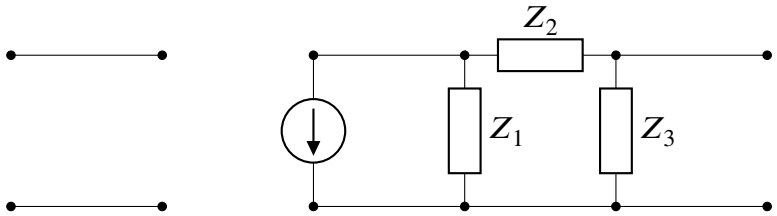


Fig. 3.19 Two-port networks for Colpitts oscillator.

By setting Z_1, Z_2, Z_3 to capacitance, inductance, and capacitance, respectively, the oscillator's transmission condition can be calculated.

When the two-terminal network of the equivalent circuit is shown in Fig. 3.19,

The ABCD matrix of these circuit components are shown as the following equations (Appendix A).

$$\hat{F}_0 = \begin{pmatrix} -\frac{1}{g_m r_0} & -\frac{1}{g_m} \\ 0 & 0 \end{pmatrix}, \tag{3.96}$$

$$\hat{F}_1 = \begin{pmatrix} 1 & 0 \\ 1/Z_3 & 1 \end{pmatrix}, \tag{3.97}$$

$$\hat{F}_1 = \begin{pmatrix} 1 & Z_2 \\ 0 & 1 \end{pmatrix}, \tag{3.98}$$

$$\hat{F}_3 = \begin{pmatrix} 1 & 0 \\ 1/Z_1 & 1 \end{pmatrix}. \tag{3.99}$$

The entire two-terminal network is written as

$$F_{\text{total}} = F_0 \dot{F}_1 \dot{F}_2 \dot{F}_3. \tag{3.100}$$

The transfer function V_o/V_s is 1/A because of its definition.

The oscillation condition is

$$V_o/V_s = 1. \tag{3.101}$$

Hense from

$$\frac{-g_m r_d Z_2 Z_1}{Z_2(Z_1 + Z_3) + r_d(Z_1 + Z_2 + Z_3)} = 1, \tag{3.102}$$

the oscillation condition is written as

$$Z_2(1 + g_m r_d)Z_1 + Z_3 + r_d(Z_1 + Z_2 + Z_3) = 0. \tag{3.103}$$

Because Z_2 and r_d are not zero,

$$(Z_1 + Z_2 + Z_3) = 0. \tag{3.104}$$

The impedances of the each component is $Z_1 = 1/j\omega C_d$, $Z_2 = 1/j\omega C_g$ and $Z_3 = j\omega L_g$. The oscillation frequency is

$$\omega = \sqrt{\frac{C_d + C_g}{L_g(C_d + C_g)}}. \tag{3.105}$$

The gain conditon for the oscillation also is written as

$$g_m r_d = \frac{C_g}{C_d}. \tag{3.106}$$

In the case of the S-parameter model, F_0 and F_3 are connected in parallel, and Γ_1 and Γ_2 are reflection coefficients (Fig. 3.20).

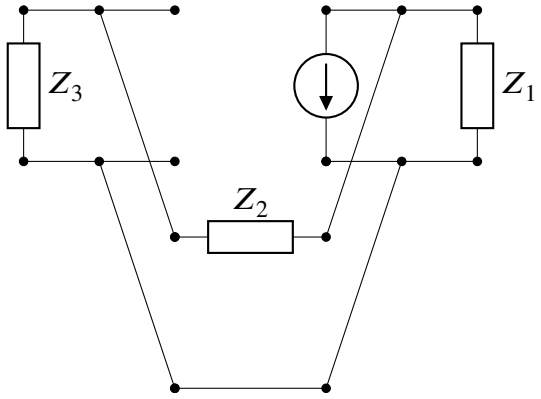


Fig. 3.20 Two-port networks for equivalent small signal model.

The oscillation condition using the S-parameter is written as

$$\begin{aligned} & 1-\left(S_{11}+\frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right) \\ & =\frac{2Z_0r_d(g_mZ_1Z_2+Z_1+Z_2+Z_3)+Z_1(Z_2+Z_3)}{(Z_0+Z_2)(r_o(g_mZ_0Z_1+Z_0+Z_1+Z_3)+Z_1(Z_0+Z_3))}. \\ & =0 \end{aligned} \tag{3.107}$$

The impedance of the circuit parameters are $Z_1 = 1/j\omega C_d$, $Z_2 = 1/j\omega C_g$,$Z_3 = j\omega L_g$, respectively. Hence, the oscillation frequency ω can be solved as

$$\omega=\sqrt{\frac{C_d+C_g}{L_g(C_d+C_g)}}, \tag{3.108}$$

using equation

$$2Z_0r_d(g_mZ_1Z_2+Z_1+Z_2+Z_3)+Z_1(Z_2+Z_3)=0, \tag{3.109}$$

where $Z_1 = 1/j\omega C_d$, $Z_2 = 1/j\omega C_g$, and $Z_3 = j\omega L_g$. The gain condition for the oscillation is also calculated as

$$g_mr_d=\frac{C_g}{C_d}. \tag{3.110}$$

These results agrees with the results calculated using the transfer function.

Chapter 4

Analysis of Oscillation phenomena of SiC MOSFETs

4.1 Oscillation phenomena of SiC MOSFETs on Type II short-circuit operation

SiC MOSFETs during short circuit operation can be unstable because of the oscillation caused by the coupling between the MOSFET and the circuit elements such as parasitic inductances, parasitic capacitances, and other MOSFETs connected in parallel. The oscillation phenomena and its suppression will be discussed in this chapter.

The test circuit shown in Fig. 4.1 is used to investigate the SiC MOSFET oscillation. A commercial 1.2 kV class SiC MOSFET C2M0080120 fabricated by CREE was used as DUT. The resistance of this device is 80mΩ. The oscillation phenomenon of the SiC MOSFET in SC Type II was investigated by turning on the high-side FET after the low-side MOSFET was turned on.

Figure 4.2 shows the gate resistance dependence of the experimental waveforms of a SiC MOSFET during SC type II. Figure 4.2(a) and 4.2(b) show the waveforms when the gate resistance of the device under test is set to 0 Ω and 15 Ω, respectively. These results show that oscillation can be caused during SC type II and it can be suppressed by increase in the gate resistance.

To analyze the oscillation condition during SC type II, the chopper type equivalent circuit shown in Fig. 4.1 is considered. L_{m} is the 100 μH load inductor. V_{ds} is a voltage power supply, which is connected to a dc link capacitor C_{ds}. V_{gs} is a signal source. R_{g1} is the gate resistance, which consists of internal and external gate resistance of M_1. L_{gs1}, L_{d1} and L_{s1}

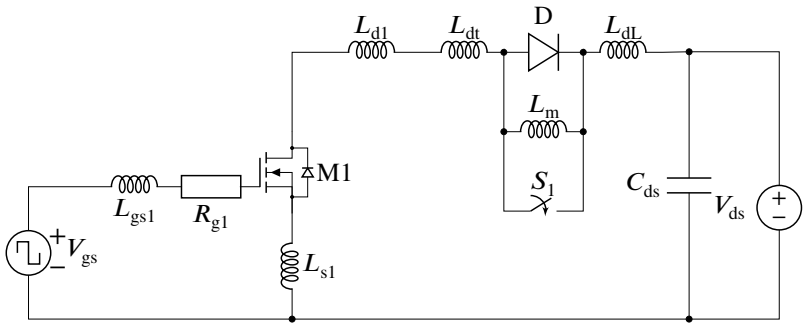
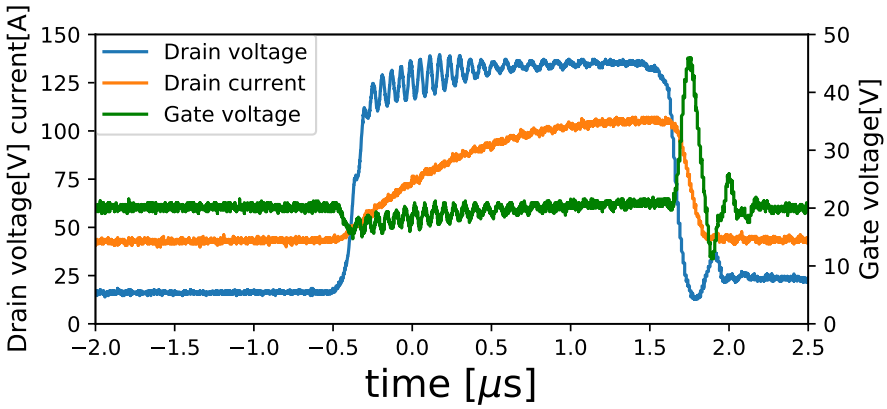
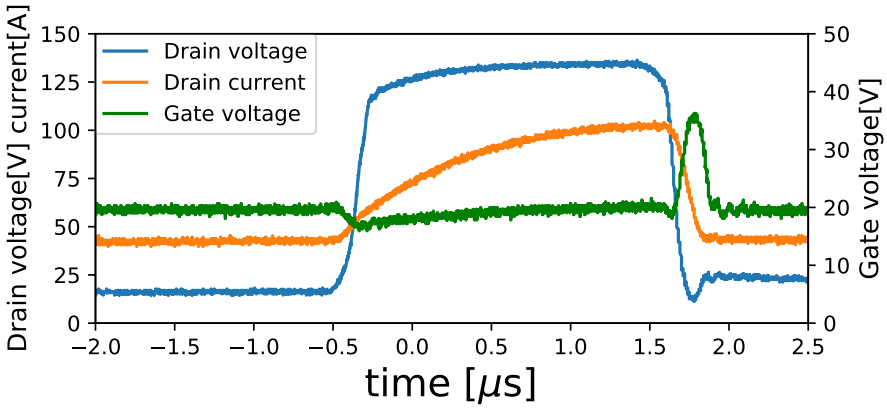


Fig. 4.1 Evaluation circuit investigated in this chapter. The circuit consists of a high-side diode and a low-side MOSFET. The ideal switch is connected in parallel with a high-side diode to reproduce SC type II in transient simulation.



(a) Waveforms for the gate resistance of 0 Ω.



(b) Waveforms for the gate resistance of 15 Ω.

Fig. 4.2 Experimental waveforms during SC type II. Commercially available SiC MOSFET (C2M0080120) was used.

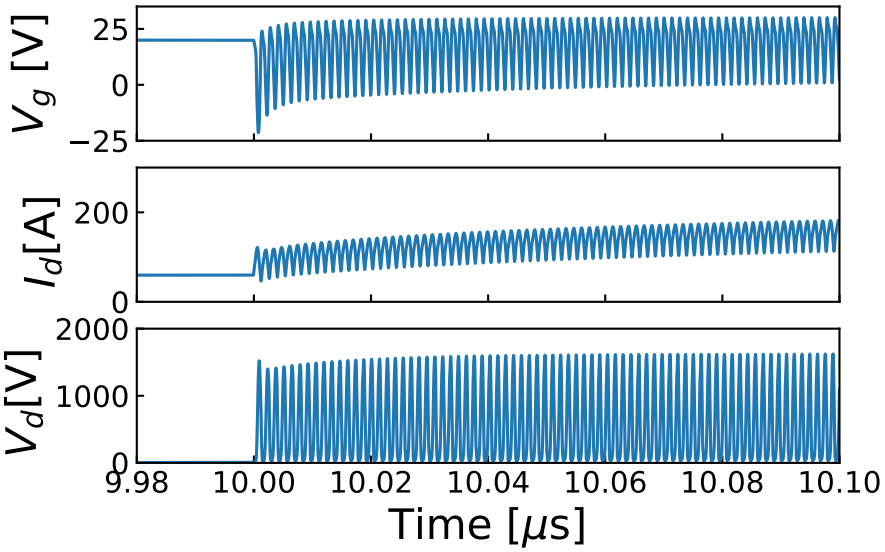


Fig. 4.3 Waveform of the gate voltage, the drain voltage and current of M1 at 10 μs using TCAD device simulation. Shortage of the high-side load causes an increase in drain voltage and continuous oscillation.

are gate, drain and source inductances, respectively. L_{dt} and L_{dL} are the inductance of the power loop. The ideal switch S_1 is connected to the high-side diode in parallel.

The switching waveforms of the circuit shown in Fig. 4.1 was calculated by mixed-mode TCAD simulation. In the calculations, the gate and drain voltages were set to 0/20 V and 600 V, respectively. To reproduce the SC type II in the simulation, S_1 was turned on after the low-side gate was turned on. For simplicity, the SPICE ideal model was adopted as the high-side diode.

Figure 4.3 shows the waveform of drain voltage, drain current, and gate voltage of M1. When the high-side switch S_1 was turned on at 10 μs, the low-side MOSFET began to oscillate. This behavior can cause circuit destruction and should be prevented by design optimization. In this case, this oscillation can be suppressed by increasing the gate resistance above 2.9 Ω. Although it can be calculated by mixed-mode TCAD simulation, it is time-consuming. Therefore, parameter optimization requires a large number of computational resources for more complex cases.

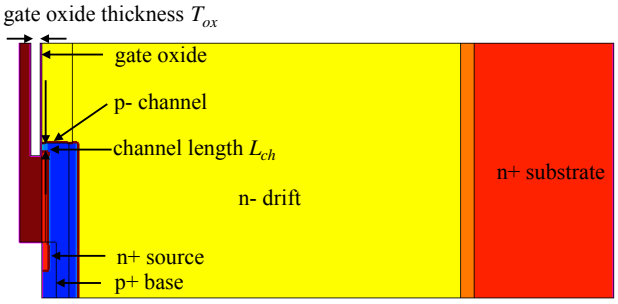


Fig. 4.4 The two-dimensional half-cell of the TCAD device model of silicon carbide MOSFET

Table 4.1 Device parameters of the TCAD device model.

L_{hcell}	4.5 μm	L_{ch}	0.3 μm
n_{ch}	5×10^{16} cm^{-3}	n_{drift}	6×10^{15} cm^{-3}
T_{ox}	50 nm	T_{drift}	15 μm

4.2 TCAD simulation model for SiC-MOSFET

4.2.1 Device structure

The TCAD device model structure for a MOSFET is shown in Fig. 4.4. The device model is modified from the structures of reference [67] and [79], which were proposed to reproduce commercial SiC MOSFETs. A lightly doped p-type region was added as a channel region of the MOSFET. Half-cell pitch L_{hcell}, channel length L_{ch}, channel doping n_{ch}, oxide thickness T_{ox}, drift layer concentration n_{drift}, and thickness T_{drift} are the device parameters. These values are shown in Table 4.1.

4.2.2 S-parameter

S-parameters under specific operating conditions can be calculated using the small-signal AC analysis function of the TCAD simulator as shown in chapter 3. In this study, the S-parameters were computed from 100 kHz to 10 GHz. Some of these results are shown in Table 4.2.

Table 4.2 S-parameter calculated by TCAD simulator.

Freqency Hz	S_{11} MAG. ANG.	S_{21} MAG. ANG.	S_{12} MAG. ANG.	S_{22} MAG. ANG.
0.10 M	0.988 -52.3	0.001 63.1	1715 153.2	0.463 -85.8
0.50 M	0.950 -135.7	0.001 21.1	705.7 111.3	0.826 -151.6
1.00 M	0.944 -156.9	0.001 10.4	372.9 100.6	0.867 -165.3
5.00 M	0.944 -174.8	0.001 -1.8	75.94 89.3	0.883 -176.7
10.0 M	0.948 -176.6	0.001 -6.6	38.00 85.4	0.886 -177.8
50.0 M	0.984 -178.1	0.001 -15.7	6.081 78.5	0.907 -178.6
100 M	0.994 -178.9	0.001 -13.2	2.816 78.8	0.913 -178.9
500 M	0.998 -179.7	0.001 -18.0	0.508 63.7	0.925 -178.2
1.00 G	0.999 -179.8	0.001 -27.4	0.221 43.8	0.943 -177.6
5.00G	1.000 -179.9	0.000 -43.7	0.015 -48.2	0.996 -178.6
10.0 G	1.000 -180.0	0.000 -44.2	0.003 -120.8	1.000 -179.4

4.3 Calculation for a single MOSFET

Stability of MOSFET during SC type II is evaluated using the oscillation condition factor $\alpha(\omega)$ introduced in chapter 3.

First, the equivalent circuit for the operation point selected is derived as follow. Since the short-circuit condition of the load is considered, the diode D on the high side and L_{m} are replaced by a short circuit. The capacitance of the power supply and the capacitance connected in parallel with the power supply are also assumed to be sufficiently large and are replaced by shorts. Then the chopper circuit presented in Fig. 4.1 can be transformed to the equivalently small-signal circuit shown in Fig. 4.5. In this equivalent ciruite, Z_{L} is defined as $Z_{\mathrm{L}} = j\omega L_{\mathrm{dL}}$.

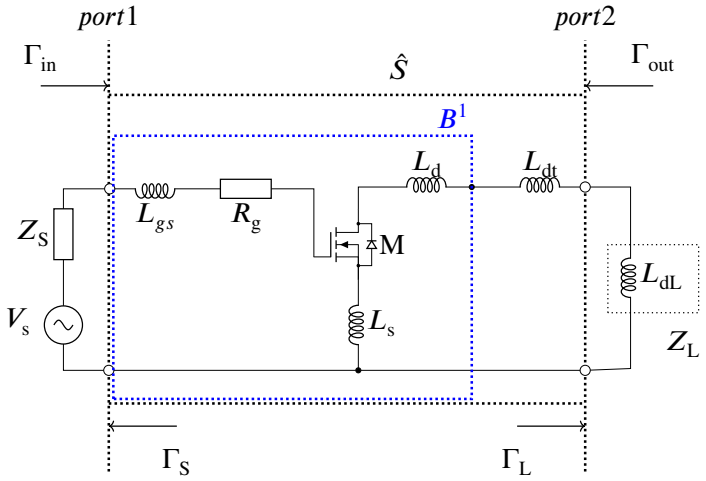


Fig. 4.5 Simplified equivalent circuit.

A signal flow graph is created using the equivalent circuit shown in Fig. 4.5 and the S-parameters. The loop gain of the device to be focused on is calculated using Mason's rule as shown in chapter 3.

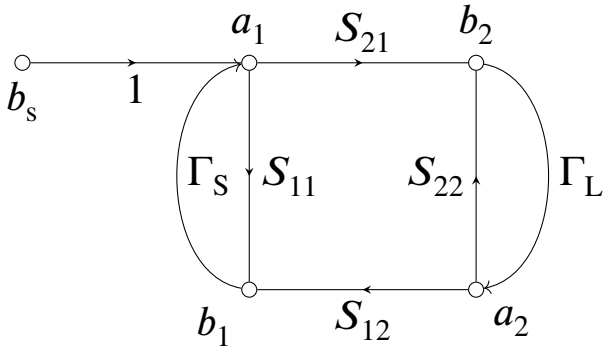


Fig. 4.6 Equivalent Signal flow graph.

Then the loop gain is written as

$$\frac{b_1}{b_s} = \frac{\Gamma_{in}}{(1-\Gamma_S\Gamma_{in})}. \tag{4.1}$$

The oscillation condition can be considered as the denominator of eq. (4.1) is zero at a particular frequency.

The oscillation condition factor is defined as

$$\alpha(\omega) = -\left(S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1-S_{22}\Gamma_L}\right)\Gamma_S\cdot, \tag{4.2}$$

in this study.

Figure 4.7 shows the gate resistance dependence of the Nyquist plot of $\alpha(\omega)$. The S-parameter of the MOSFET is calculated at $V_d = 600$ V and $V_g = 20$ V with TCAD simulation. As the gate resistance R_{g1} increases from 1.0 Ω to 11.9 Ω, the intersection of the plotted line and the imaginary axis moves from left to right of (-1, 0j). The intersection represents the intensity of the loop gain. Thus, the oscillation is suppressed when the intersection is to the right of (-1, 0j). The gate resistance when the intersection is at (-1, 0j) is defined as the critical resistance.

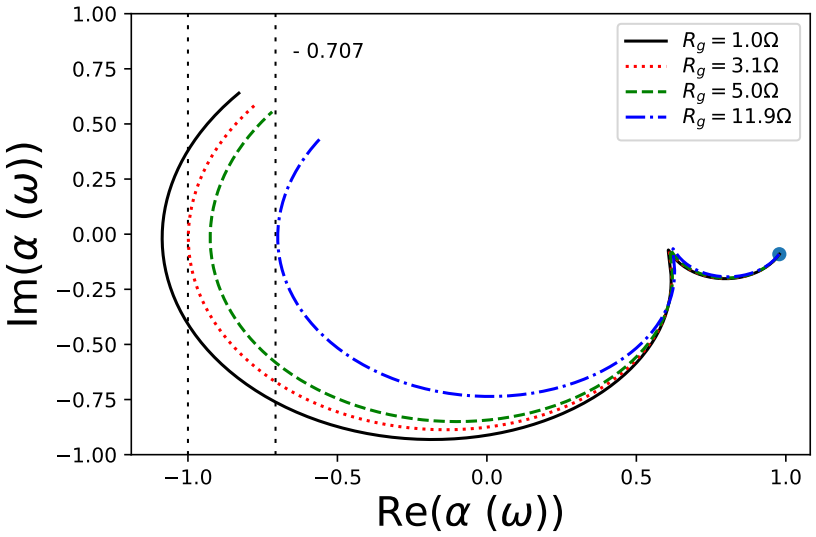


Fig. 4.7 The Nyquist plot of the oscillation condition factors $\alpha(\omega)$.The circuit parameters are set as $L_{s1} = 10$ nH, $L_{gs1} = 1$ nH, $L_{dL} = 1$ nH, and $L_{dt} = 1$ nH. These plots show the calculated results when ω changes from 100 kHz to 1 GHz. The circle points indicate the calculation results at 100 kHz.

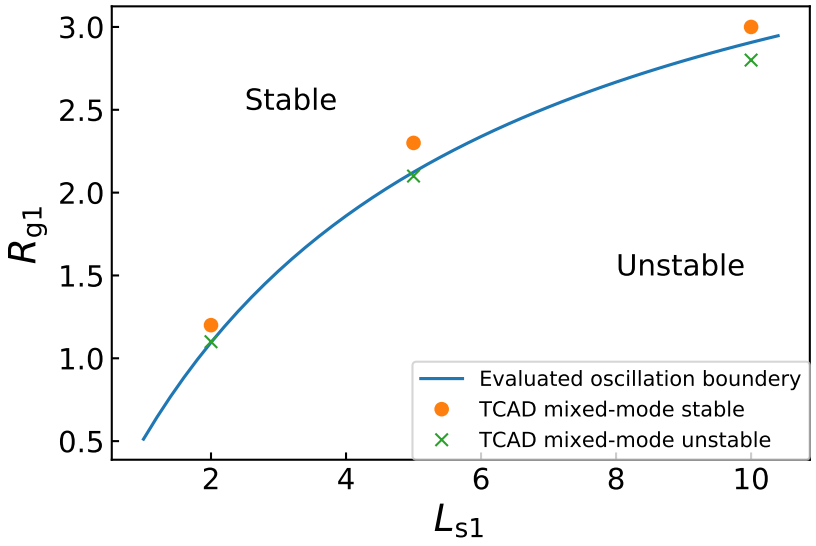


Fig. 4.8 L_{s1} dependence of the external resistance (R_{g1}) to suppress the oscillation. The line represents the boundary between the stable and unstable regions. The circles and crosses are the results of the TCAD simulation, which indicate where the oscillation was suppressed and occurred, respectively.

Figure 4.8 shows the critical gate resistance dependence on the source inductance. The result calculated from equation (3.58) is indicated by the solid line. The left- and right-hand

side of the line represent the stable region, and the region where oscillation occurs, respectively. The same graph shows the results calculated using a mixed-mode TCAD transient simulation. The crosses indicate points where oscillation has occurred, and the circles indicate points where oscillation has been suppressed. In the TCAD simulations, if the amplitude of the gate oscillation tends to continue or increase at 50 ns or 100 ns from the start of SC, the condition is determined as unstable.

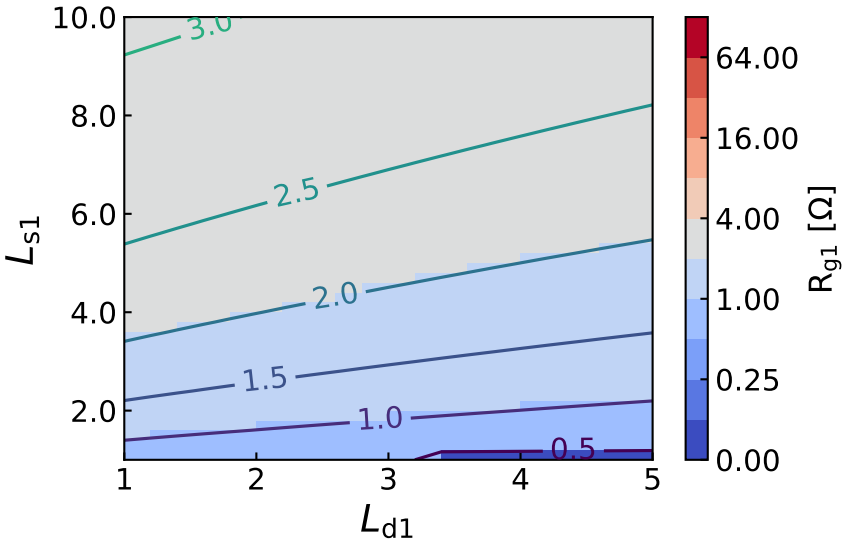


Fig. 4.9 The critical resistance (R_{g1}) to suppress the oscillation evaluated by the oscillation condition factors $\alpha(\omega)$. The circuit parameters are set as $L_{dL} = 1$ nH, $L_{gs1} = 2$ nH, and $L_{dt} = 1$ nH.

In the R_{g1} and L_{s1} dependence of the oscillation, the boundary between the oscillation and non-oscillation regions calculated by the proposed method is consistent with the transient analysis results of the TCAD simulation. The proposed method enables us to estimate the device and circuit parameters required to suppress oscillation.

Figure 4.9 shows the dependence of the critical gate resistance on L_{d1} and L_{s1}. The critical gate resistance differs depending on the circuit parameters. From this graph, the critical gate resistance decreases as L_{d1} increases. This shows that the circuit is changing in a stable direction. In contrast, when L_{s1} is increased, the circuit becomes unstable because the critical gate resistance increases.

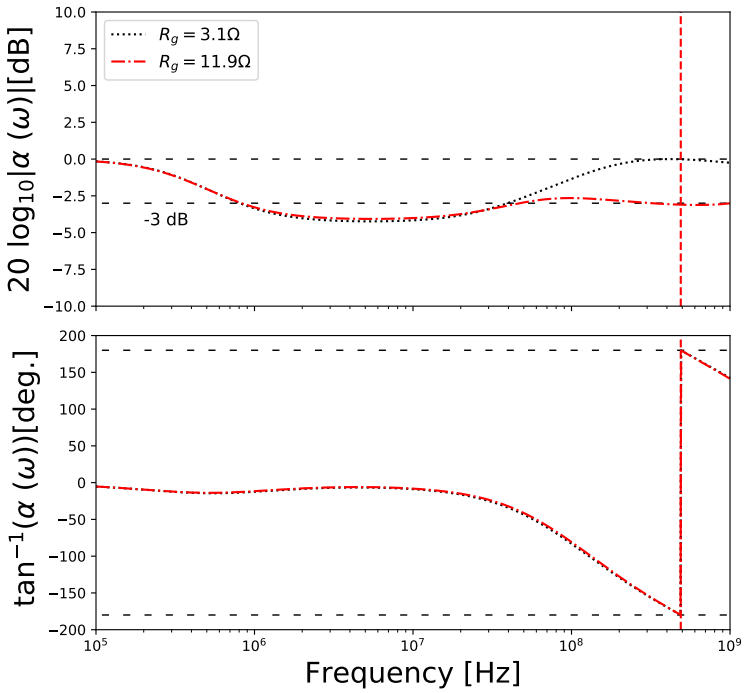


Fig. 4.10 Bode diagram of the oscillation factor $\alpha(\omega)$. The phase and gain of the loop gain are -180˚ and 0 db respectively, when $R_{g1} = 3.1\ \Omega$. In contrast, the phase and gain of the loop gain are -180˚ and -3 db respectively when $R_{g1} = 11.9\ \Omega$.

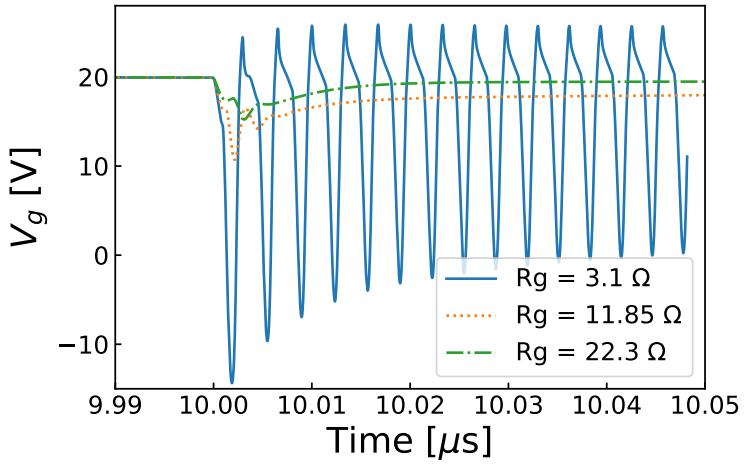


Fig. 4.11 Gate resistance dependence of the gate voltage waveform. When $R_{g1} = 3.1$, 11.9, and 22.3 Ω, the gain corresponds to 0 dB, -3 dB, and -6 dB, respectively.

In an actual design, some gain margin is required. Figure 4.10 presents the resistance dependence of the loop gain and phase. The points at which the phase shift becomes -180˚ are 430 MHz for each resistor. When Rg = 3 Ω, the loop gain is 0 dB at 430 MHz. This is the

critical resistance when the oscillation occurs or not. Conversely, when the gate resistance is 11.9 Ω, the loop gain at 430 MHz becomes -3 dB.

Figure 4.11 shows the gate voltage waveforms calculated with the mixed-mode TCAD transient simulation. The waveform changes depending on R_{g1}. The gate resistances of 11.9 and 22.3 Ω correspond to gain margins of -3 db and -6 db, respectively. From this result, the sufficient damping effect is obtained by the gain margin of -3 db in this case.

4.4 Calculation for parallel connected SiC MOSFETs

4.4.1 Signal flow model for MOSFETs connected in parallel

In this section, oscillation in a circuit in which MOSFETs are connected in parallel will be considered. Because MOSFETs are generally connected in parallel in high-power modules, it is necessary to evaluate the circuit parameters for a stable operation on the circuit. Feedback signal loops via parallel-connected MOSFETs can reduce the stability of the circuit compared to the circuit consisting of the single MOSFET described above. The stability analysis method for parallel connection will be carried out using a chopper circuit as shown in Fig. 4.12. The circuit consists of one high-side diode and two low-side MOSFETs connected in parallelly. The active areas of the MOSFETs are half of the single MOSFET as shown in Fig. 4.1. Parasitic capacitance and mutual inductance of the package are ignored in this equivalent circuit, they can be considered by using the S-parameter obtained from, simulations and analytical calculations using the proposed method. The stability in the SC type II operation will also be discussed.

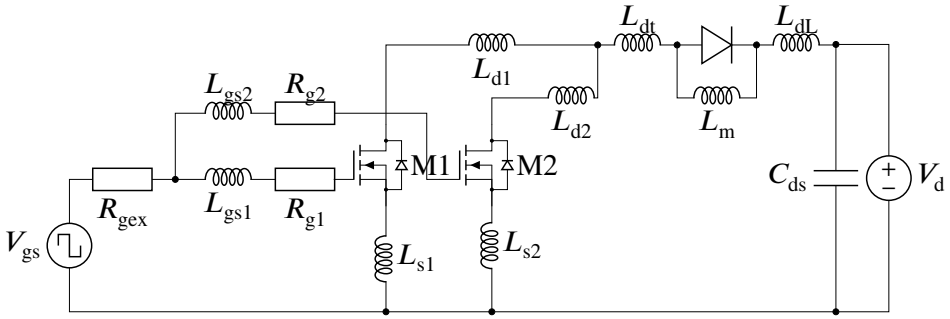


Fig. 4.12 Evaluation circuit used to calculate oscillation conditions when MOSFETs are connected in parallel.

Figure 4.13 shows the equivalent circuit model in which the diode, signal source and load are modeled similar to that of a single device. The difference from the single-device case is that the MOSFETs are connected parallelly.

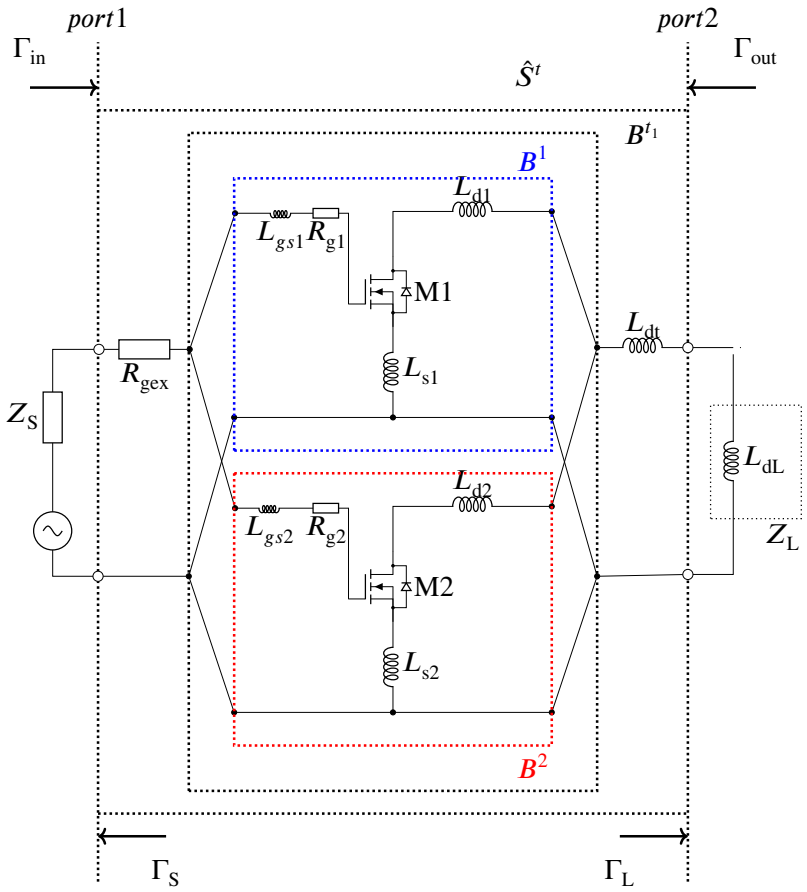


Fig. 4.13 Simplified small signal equivalent circuit

The oscillation condition factor $\alpha(\omega)$ can be applied to a multi-chip case. The S-parameter of a multi-chip circuit $\hat{S}^t$ can be computed from TCAD simulation results of the MOSFET as shown in eq. (3.87). When we use $\hat{S}^t$, oscillation condition factor $\alpha(\omega)$ can be written as

$$\alpha(\omega) = -\left(S^t_{11} + \frac{S^t_{12} S^t_{21} \Gamma_{\mathrm{L}}}{1 - S^t_{22} \Gamma_{\mathrm{L}}} \right) \Gamma_{\mathrm{S}}, \tag{4.3}$$

where Γ_{S} and Γ_{L} are the input and the load reflection coefficient, respectively.

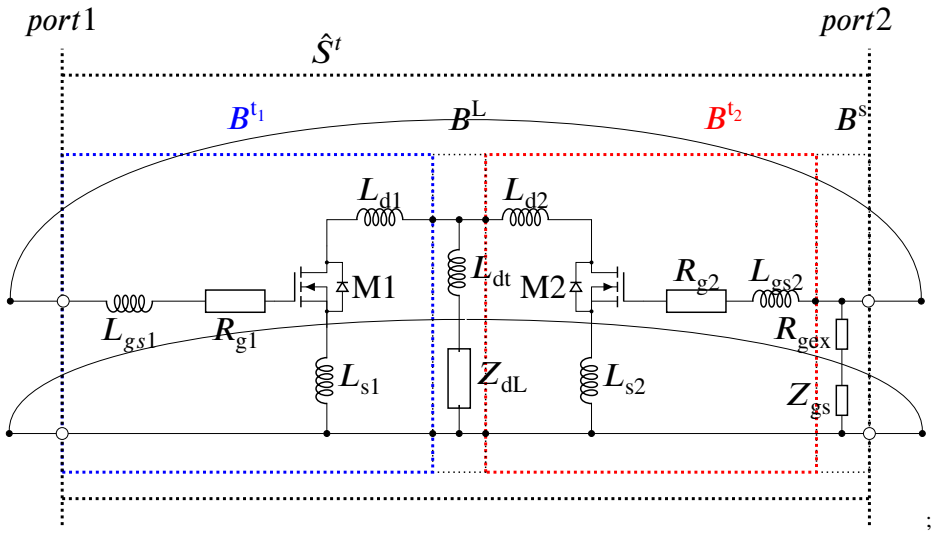
The oscillation condition factor $\alpha(\omega)$ can only compute the common oscillation mode. When MOSFETs are symmetrically connected and with low impedance, the oscillation can be induced by differential oscillation mode[49, 48]. To compute this mode, the other oscillation condition factor $\beta(\omega)$ introduced in chapter 3 is used. Figure 3.16(a) and 3.16(b) show the equivalent circuit and the signal flow graph of this oscillation mode. In this equivalent circuit, the input signal is transferred through the drain of MOSFETs to the gate of the second MOSFET. After the signal passes through the gate of the second MOSFET, the signal is fed back to the gate signal of the first MOSFET.

To compute the stability of the circuit, a virtual ground and virtual signal source at port 1 are set as shown in Fig. 3.16(a). b_{s} is the virtual input signal. a_1, b_1, a_2, and b_2 are power waves. $\hat{S}^t$ is an S-parameter of two-port network consisting of power MOSFETs and passive components as shown in Fig. 3.16(a). $\hat{S}^t$ can be computed from the TCAD simulation results of the MOSFET using the signal flow-graph analysis technique. The oscillation condition of the circuit can be written as

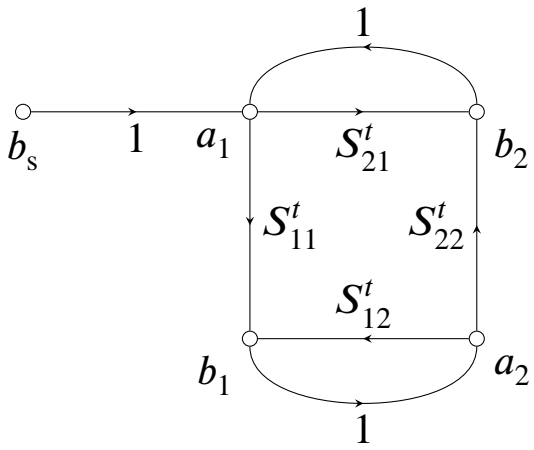
$$1 - \left(S^t_{21} + \frac{S^t_{11} S^t_{22}}{1 - S^t_{12}} \right) = 0. \tag{4.4}$$

To compute the oscillation condition, the Nyquist stability condition is used. The oscillation condition factor is introduced as

$$\beta(\omega) = -\left(S^t_{21} + \frac{S^t_{11} S^t_{22}}{1 - S^t_{12}} \right). \tag{4.5}$$



(a) Simplified small signal equivalent circuit

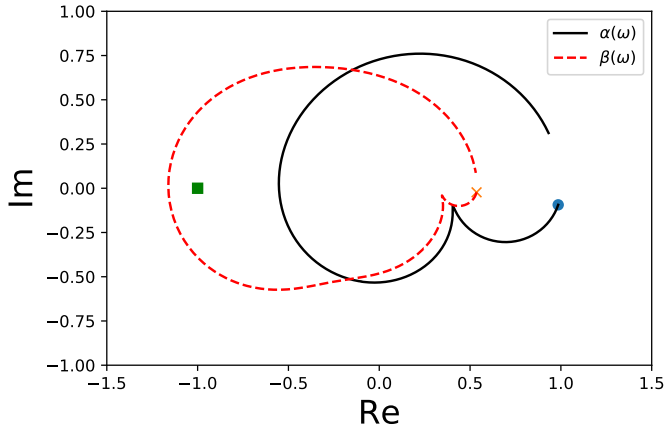


(b) Signal flow graph

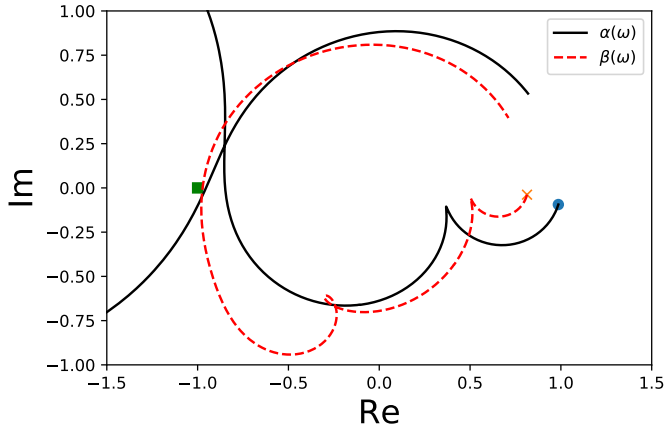
Fig. 4.14 Simplified equivalent circuit and signal flow graph to evaluate the oscillation condition.

4.4.2 Calculation results of oscillation of MOSFETs connected in parallel

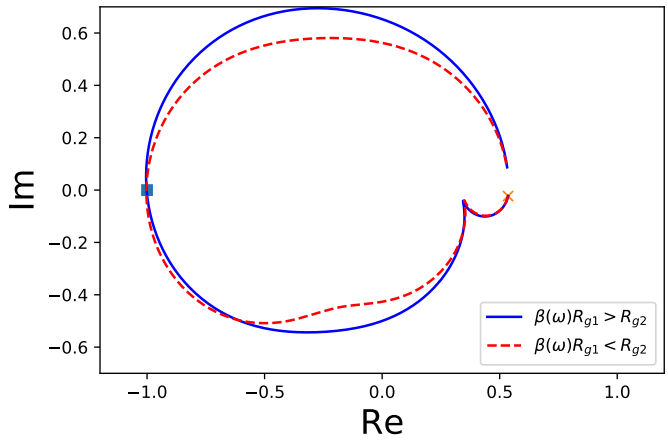
Figure 4.15(a) shows the Nyquist plot with $\alpha(\omega)$ and $\beta(\omega)$ whose circuit parameters are set as $L_{d1} = L_{d2}$, $L_{s1} = L_{s2}$, and $L_{gs1} = L_{gs2}$. The Nyquist plot with $\beta(\omega)$ moves to the left-hand side of the point (-1, $0j$). In contrast, the Nyquist plot with $\alpha(\omega)$ moves to the right-hand side of the point (-1, $0j$). Therefore, the oscillation condition $\beta(\omega)$ determines the stability of the circuit. This result reveals that inter-chip oscillation tends to occur when MOSFETs are connected symmetrically in parallel.



(a) The circuit parameters are set as $L_{d1} = L_{d2} = 5$ nH, $L_{gs1} = L_{gs2} = 5$ nH, and $R_{gex} = 15.0\ \Omega$. $R_{g1} = R_{g2} = 3.0\ \Omega$.



(b) The circuit parameters are set as $L_{d1} = 1$ nH, $L_{d2} = 5$ nH, $L_{gs1} = 1$ nH, $L_{gs2} = 5$nH, and $R_{gex} = 5.0\ \Omega$. $R_{g1} = R_{g2} = 3.0\ \Omega$.



(c) The circuit parameters are set as $L_{d1} = L_{d2} = 5$ nH, $L_{gs1} = L_{gs2} = 5$nH, and $R_{gex} = 15.0\ \Omega$. The blue line shows $\beta(\omega)$ when $R_{g1} = 2.0$ and $R_{g2} = 8.0\ \Omega$. The red dotted line shows $\beta(\omega)$ when $R_{g1} = 8.0$ and $R_{g2} = 2.0\ \Omega$.

Fig. 4.15 The Nyquist plot with the oscillation condition factors when the circuit parameters are set as $L_{s1} = L_{s2} = 10$ nH, $L_{dt} = 1$ nH. These plots show the calculated results when ω changes from 100 kHz to 10 GHz. The circles and cross points indicate the results of the calculation at 100 kHz. The square points indicate the point (-1, 0j).

Figure 4.15(b) shows the Nyquist plot with $\alpha(\omega)$ and $\beta(\omega)$ oscillation condition factors when the circuit parameters are set as $L_{gs1} < L_{gs2}$, $L_{\mathrm{d1}} < L_{\mathrm{d2}}$, $L_{\mathrm{s1}} = L_{\mathrm{s2}}$, and $R_{\mathrm{g1}} = R_{\mathrm{g2}}$. The Nyquist plot with $\alpha(\omega)$ moves to the left-hand side of the point (-1, $0j$). In contrast, the Nyquist plot with $\beta(\omega)$ moves to the right-hand side of the point (-1, $0j$). Therefore, the oscillation condition $\alpha(\omega)$ determines the stability of the circuit. This result implies that common mode oscillation tends to occur when the MOSFETs are connected asymmetrically in parallel.

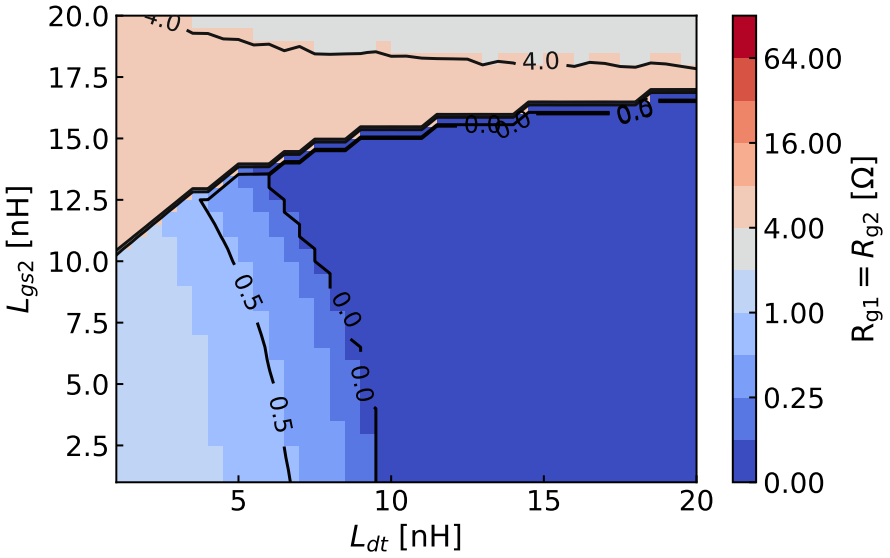
Figure 4.15(c) shows R_{g1} and R_{g2} dependence of the Nyquist plot with $\beta(\omega)$ oscillation condition factors when the circuit parameters are set as $L_{gs1} = L_{gs2}$, $L_{\mathrm{d1}} = L_{\mathrm{d2}}$, $L_{\mathrm{s1}} = L_{\mathrm{s2}}$. The blue line shows $\beta(\omega)$ when $R_{\mathrm{g1}} = 2.0\ \Omega$ and $R_{\mathrm{g2}} = 8.0\ \Omega$. The red dotted line shows $\beta(\omega)$ when $R_{\mathrm{g1}} = 8.0\ \Omega$ and $R_{\mathrm{g2}} = 2.0\ \Omega$. Comparison between $\beta(\omega)$ of $R_{\mathrm{g1}} > R_{\mathrm{g2}}$ and $\beta(\omega)$ of $R_{\mathrm{g1}} < R_{\mathrm{g2}}$ shows that the exchange of the order of R_{g1} and R_{g2} does not affect the derivation of the critical resistance. When other parameters are different, such as $L_{\mathrm{gs1}} > L_{\mathrm{gs2}}$, the exchange of the order of devices also does not affect the derivation of the critical resistance. In the following discussion we will consider the case where $R_{\mathrm{g1}} = R_{\mathrm{g2}}$.

Figure 4.16(a) and 4.16(b) show the critical gate resistance (R_{g1}= R_{g2}) evaluated with the oscillation condition factors $\alpha(\omega)$ and $\beta(\omega)$ when the circuit parameters are set as L_{d1} = L_{d2} = 2 nH, $L_{\mathrm{s1}} = L_{\mathrm{s2}}$ = 10 nH, L_{gs1} = 2 nH, L_{dL} = 1, L_{dt} = 1 nH, and R_{gex}= 1.5 Ω. In these results, the region indicated as $R_{\mathrm{g1}} = R_{\mathrm{g2}} = 0\ \Omega$ satisfies the Nyquist stability condition when $R_{\mathrm{g1}} = R_{\mathrm{g2}} > 0$. Thereore, there is no oscillation in the area.

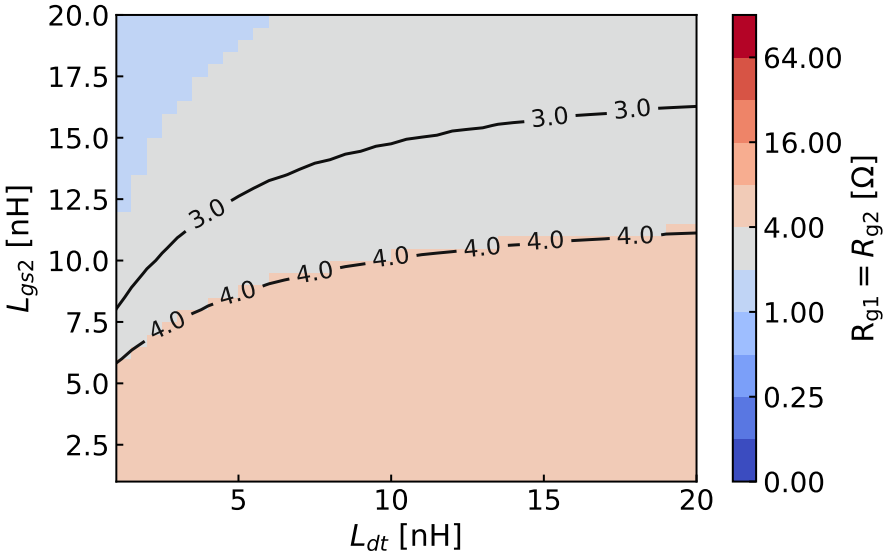
In Fig. 4.16(a), in the region where L_{gs2} is smaller than 15nH, the circuit becomes more stable as L_{dt} is increased. However, there exists a region where the circuit becomes unstable even when L_{gs2} assumes the values around 17 nH. This region becomes smaller as L_{dt} increases. In Fig. 4.16(b), a larger damping resistance is required as L_{gs2} is decreased.

In order to investigate the oscillation when L_{gs2} is approximately 17 nH, the dependence of the critical resistance on L_{gs2} and L_{d2} when L_{d} = 1 nH was evaluated. Figure 4.17(a) and 4.17(b) show the critical resistance of $R_{\mathrm{g1}} = R_{\mathrm{g2}}$ computed with the oscillation factor $\alpha(\omega)$ and $\beta(\omega)$ when L_{d2} and L_{gs2} are used as parameters. As L_{d2} increases, the region of L_{gs2} where the circuit becomes stable decreases. This result implies that the loop through the feedback capacitance and the inductance of L_{gs2} and L_{d2} contribute to this oscillation mode. Although optimizing L_{d2}, L_{gs2} and L_{dt} can suppress oscillation, its applicable range is limited because of the trade-off relationship with increasing surge voltage.

It is also possible to suppress oscillation in this mode by increasing the R_{gex}. However, as the total resistance per chip increases, the switching loss increases. Therefore, the increase in total gate resistance should be minimized.

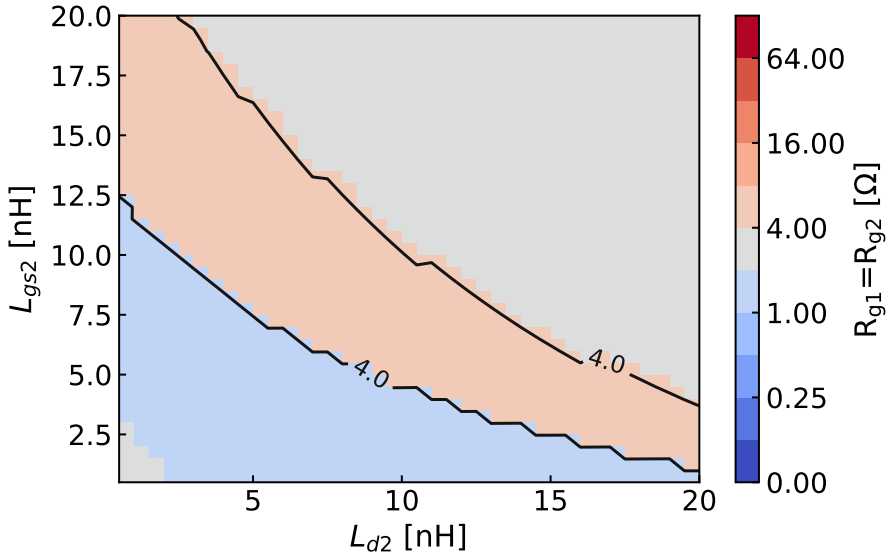


(a) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\alpha(\omega)$.

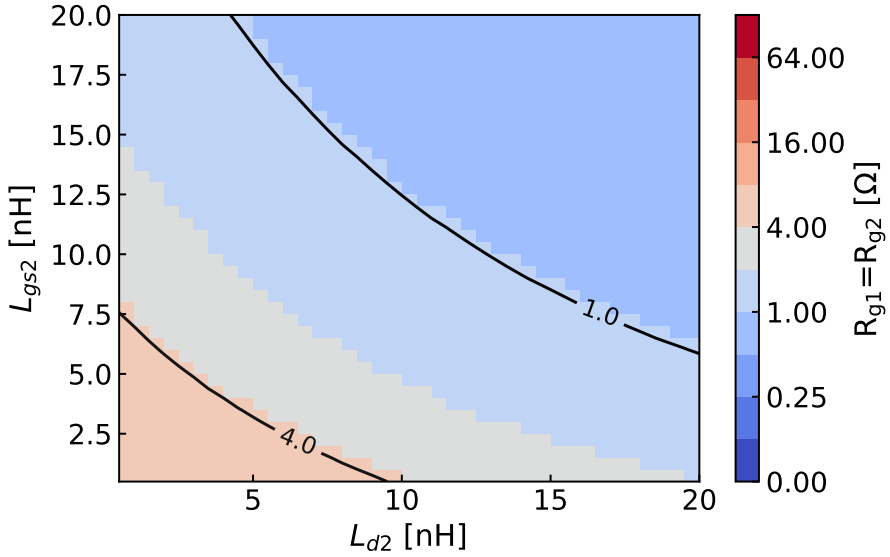


(b) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\beta(\omega)$

Fig. 4.16 Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by the oscillation condition factors $\alpha(\omega)$ and $\beta(\omega)$. The circuit parameters are set as $L_{d1} = L_{d2} = 2$ nH, $L_{s1} = L_{s2} = 10$ nH, $L_{gs1} = 2$ nH, $L_{dL} = 1$ nH, and R_{gex}= 1.5 Ω.

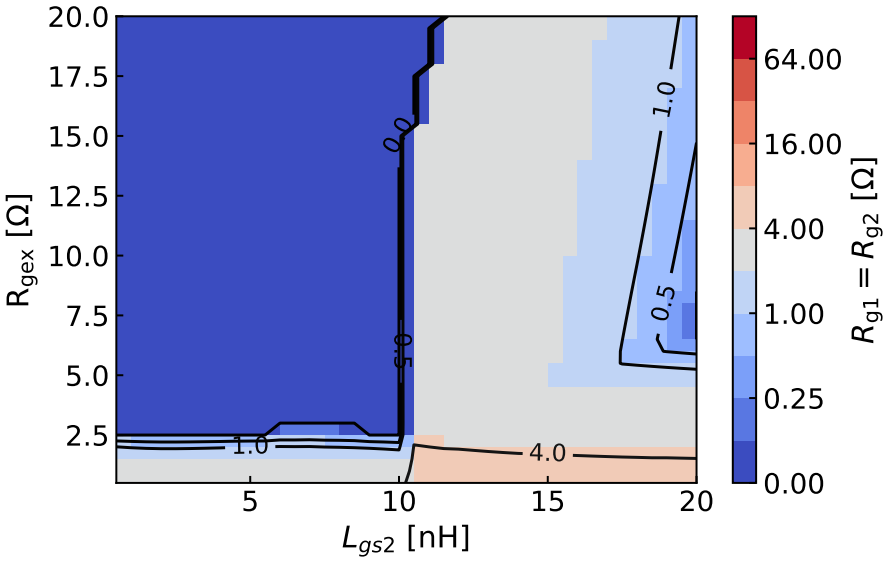


(a) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\alpha(\omega)$.

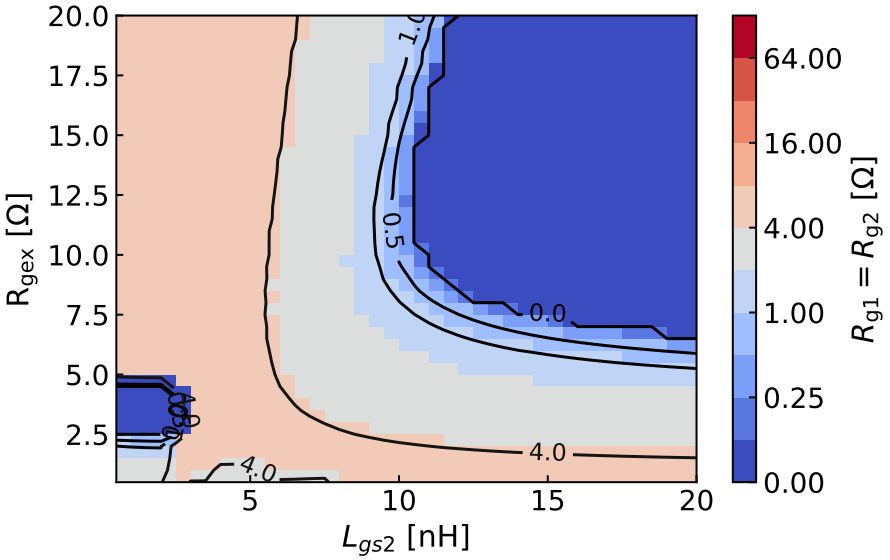


(b) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\beta(\omega)$.

Fig. 4.17 Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by the oscillation condition factors $\alpha(\omega)$ and $\beta(\omega)$. The circuit parameters are set as $L_{d1} = 2$ nH, $L_{s1} = L_{s2} = 10$ nH, $L_{gs1} = 2$ nH, $L_{dL} = 1$, $L_{dt} = 1$ nH, and $R_{gex} = 1.5$ Ω.



(a) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\alpha(\omega)$.



(b) Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by oscillation condition factors $\beta(\omega)$.

Fig. 4.18 Critical gate resistance ($R_{g1} = R_{g2}$) evaluated by the oscillation condition factors $\alpha(\omega)$ and $\beta(\omega)$. The circuit parameters are set as $L_{d1} = L_{d2} = 2$ nH, $L_{s1} = L_{s2} = 10$ nH, $L_{gs1} = 2$ nH, $L_{dL} = 1$ nH, and $L_{dt} = 1$ nH.

Figures 4.18(a) and 4.18(b) show the critical resistance of $R_{g1} = R_{g2}$ computed using $\alpha(\omega)$ and $\beta(\omega)$, respectively. In Fig. 4.18(a), the resistance required for oscillation suppression decreases as R_{gex} increases. Especially in the range of $L_{gs2} < 10$ nH and $R_{gex} > 2.5$ Ω, R_{g1} and R_{g2} are not necessary for oscillation suppression. In Fig. 4.18(b), the critical

resistance is decreased by adding R_{gex} when $L_{\mathrm{gs2}} > 10$ nH. In contrast, in the range of $L_{\mathrm{g}} < 10$ nH, the increase of R_{gex} is not effective in reducing the critical resistance.

For actual design, it is necessary to have several gain margins. Figure 4.19 shows the total gate resistance perchip $2 \times R_{\mathrm{gex}} + R_{\mathrm{g1}}$ to suppress oscillation with a 3 dB gain margin computed using $\alpha(\omega)$ and $\beta(\omega)$. As R_{gex} is increased, the critical resistances obtained from $\alpha(\omega)$ and $\beta(\omega)$ are both reduced. The total resistance required for oscillation suppression, which is determined by $\alpha(\omega)$, has a minimum value when R_{gex} is 1.5 Ω. In contrast, the R_{gex} dependence of the critical resistance determined by $\beta(\omega)$ is small, and the total resistance monotonically increases with an increase in R_{gex}.

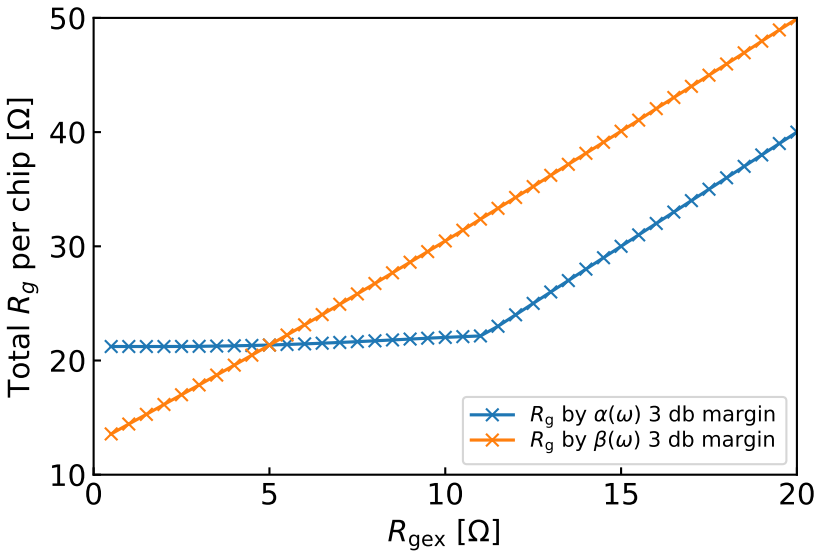


Fig. 4.19 Total gate resistance par chip evaluated by oscillation condition factors $\alpha(\omega)$ and $\beta(\omega)$ with 3 db gain margin. The circuit parameters are set as $L_{\mathrm{d1}} = L_{\mathrm{d2}} = 2$ nH, $L_{\mathrm{s1}} = L_{\mathrm{s2}} = 10$ nH, $L_{\mathrm{gs1}} = 2$ nH, $L_{\mathrm{gs2}} = 5$ nH, $L_{\mathrm{dL}} = 1$, and $L_{\mathrm{dt}} = 1$ nH.

As described above, the proposed method is simple; however, it can be used to determine the circuit parameters required for oscillation suppression. For oscillation suppression under SC conditions, it is effective to reduce the source inductance and increase the drain inductance. In addition, by increasing the gate resistance of each FET, the inter-chip oscillation can be reduced. The proposed method enables us to optimize the total resistance required for oscillation suppression.

4.5 Summary

In this chapter, the oscillation phenomena in SiC MOSFET are investigated using the method introduced in chapter 3 to evaluate oscillation condition. The proposed method can be used to evaluate the oscillation condition depending on the device and circuit parameters during the SC type II through a simple calculation using a signal flow method and S-parameter, computed using TCAD device simulation. Parameter optimization against the oscillation phenomena has been simplified compared with the mixed-mode simulation.

For devices that can operate at high speed, such as SiC MOSFETs, chip-to-chip oscillation may occur when multiple devices are connected, even if optimization is performed for a single-device design. In this case, it is necessary to increase the gate resistance to stabilize the circuit operation because the device parameters have already been determined. If the gate resistance and overall device and circuit parameters can be adjusted, the trade-off between loss and stable circuit operation can be improved. This method enables the optimization of device and circuit parameters from the initial stage of module design. Furthermore, it is a useful method for the power device, gate driver, and package design.

Chapter 5

Analysis of Oscillation phenomena of Si-IGBTs

In this chapter, the oscillation phenomena of Si-IGBTs under short circuit Type II conditions are experimentally measured and analyzed using the proposed method. The electron-hole plasma inside the device can also be the origin of oscillation phenomena in IGBTs, unlike SiC-MOSFETs described in the previous chapters. The relationship between the internal carrier response of the IGBT and oscillation phenomena are investigated in this chapter.

5.1 Oscillation phenomena of Si IGBTs on short-circuit Type II operation

5.1.1 Experiment for oscillation on Type II short circuit operation

Figure 5.1 shows the circuit used in the experiments to investigate the oscillation phenomena in the SC type II. Commercial Si-IGBTs (Infineon IGW08T120FKSA1 1200 V, 16 A) were used as the device under test (DUT). L_G, L_E, L_C, L_{DC} are stray inductances, and L_m is the load inductance. These values are determined by measurements using an impedance analyzer and the switching waveform comparison.

An Si-IGBT module (Mitsubishi electric CM400DY-34T, 1700 V, 400 A) with a sufficiently high rated current was used as the high-side switch S_1. The experiments were conducted at room temperature. The driving gate voltage was 20/-5 V. The gate resistance R_G and collector voltage V_{DC} are variable. Table 5.1 shows the evaluated parameters. To reproduce the SC type II, S_1 was turned on while the low-side gate was turned on.

Table 5.1 TCAD device parameters shown in Fig.5.5.

L_G	L_C	L_{DC}	L_E	L_m
200 nH	5 nH	20 n H	20 nH	100 uH
R_G	V_{Drive} on	V_{Drive} off	V_{DC}	C_{DC}
variable	20 V	-5 V	variable	100 μ F

Figure 5.2 shows the switching waveforms of the IGBT in SC type II when $V_{DC} = 100$ V and $R_G = 3.3$ Ω. It can be seen from Fig. 5.2 that the short-circuit event induced the gate voltage, the collector voltage and the collector current oscillations. This oscillation was affected by the collector voltage. Figure 5.3 shows the switching waveforms when $V_{DC} =$ 100 V, $R_G = 3.3$ Ω and $V_{DC} = 600$ V, $R_G = 1.2$ Ω. Under each condition, the gate and drain voltages oscillation occurred in SC type II when $V_{DC} = 100$ V and 600 V, respectively. The oscillation frequencies were 9.2 and 15.1 MHz when $V_{DC} = 100$ V and 600 V, respectively.

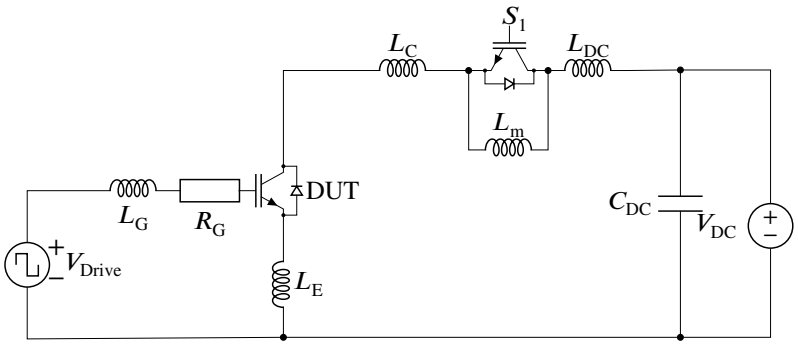


Fig. 5.1 Evaluation circuit investigated in this study. The circuit consists of a high-side IGBT with a parallel connected fast recovery diode and a low-side IGBT.

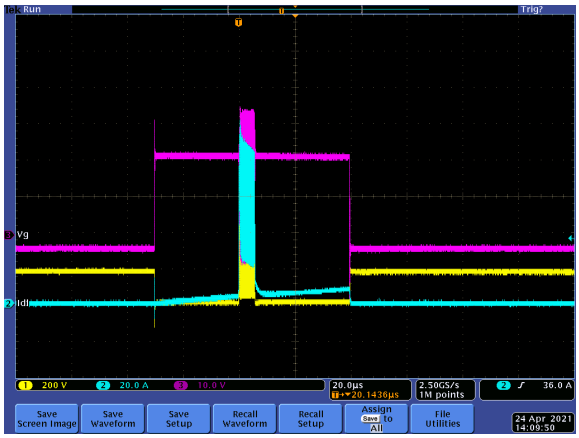
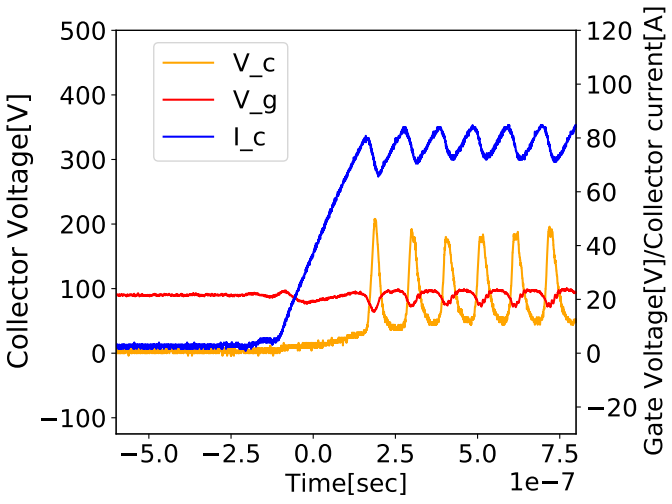
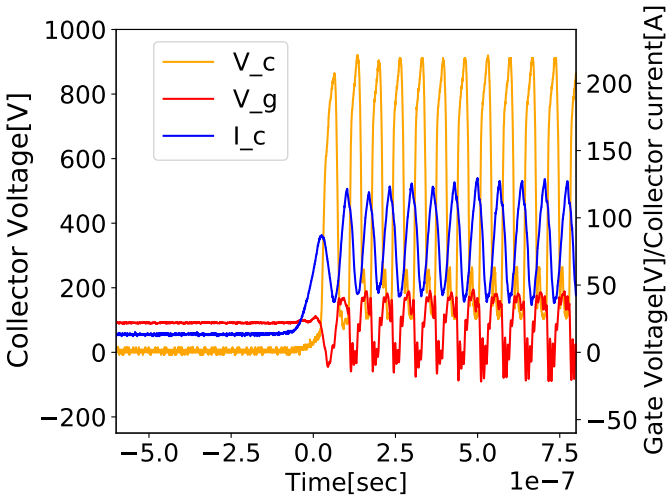


Fig. 5.2 Switching waveforms of the IGBT in SC type II. The high-side switch was turned on during low-side IGBT.



(a) $V_c = 100$ V



(b) $V_c = 600$ V

Fig. 5.3 Enlarged switching waveforms of the IGBT in SC type II. The high-side switch was switched on while the low-side IGBT was on. The short-circuit current induced a parasitic oscillation of the IGBT.

These oscillations can be suppressed by increasing the gate resistance. Figure 5.4 shows the presence of oscillations depending on the gate resistance and collector voltage. The circles indicate the points that oscillation was not observed, and crosses indicate the points that oscillation was observed. The gate resistance required to suppress the oscillation increased with decreasing collector voltage. Based on this result, oscillation is more likely to occur as the collector voltage decreases.

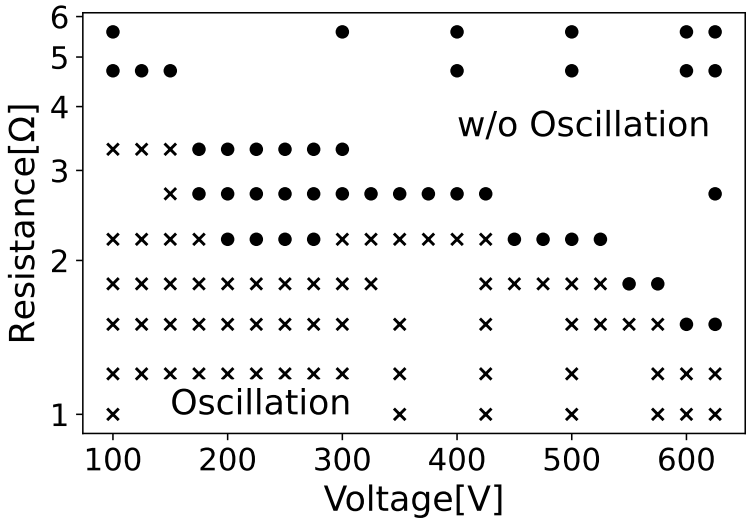


Fig. 5.4 Dependence of the occurrence of oscillation on gate resistance and collector voltage. The circles indicate the points that oscillation was not observed, and crosses indicate the points that oscillation was observed.

5.2 TCAD simulation model for Si-IGBT

To investigate the oscillation phenomena of the Si-IGBT, the signal flow method and S-parameter computed from TCAD device simulation introduced in chapter 3 are adopted.

A TCAD simulation model is introduced to calculate the oscillation condition factor $\alpha(\omega)$. An IGBT with a trench field-stop structure [80, 81] was used as IGW08T120. The detailed design parameters of the IGBT were unclear because it was a commercial product. Thus, the structure shown in Fig. 5.5 was assumed.

The device parameters were determined by referring to previous studies on the simulation model analysis for trench field stop IGBTs [82] and by comparing the calculation results with the characteristics provided in the datasheet [83]. The I_c-V_c characteristics were calculated based on these parameters in Fig. 5.6. The on-voltage calculated of 1.7 V using TCAD simulation is equivalent to that in the datasheet. The calculated saturation current characteristic at high voltage is approximately 100 A, which is similar to the saturation current in the SC test. The calculated capacitance characteristics are shown in Fig. 5.7. The calculated curves shows agreement with the capacitance values in the data sheet. Table 5.1 lists the device parameters of the TCAD device model.

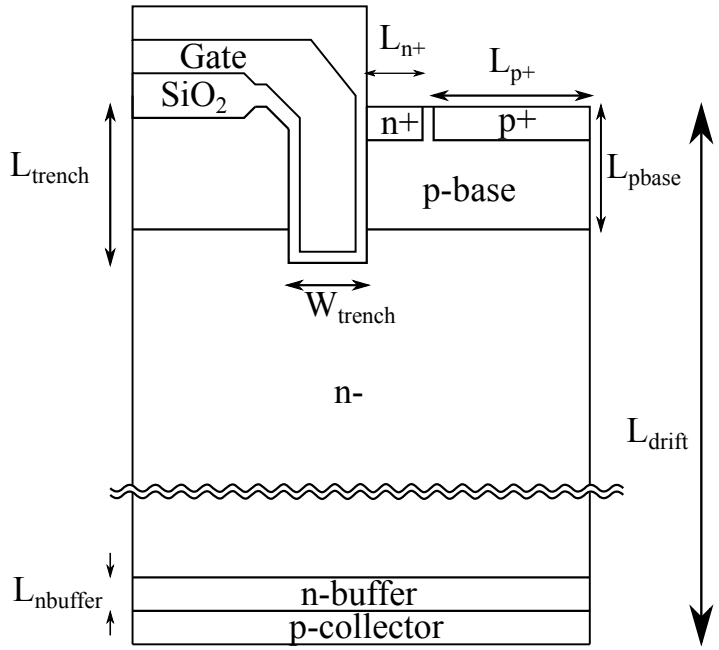


Fig. 5.5 Schematic of simulation model structure of the trench IGBT.

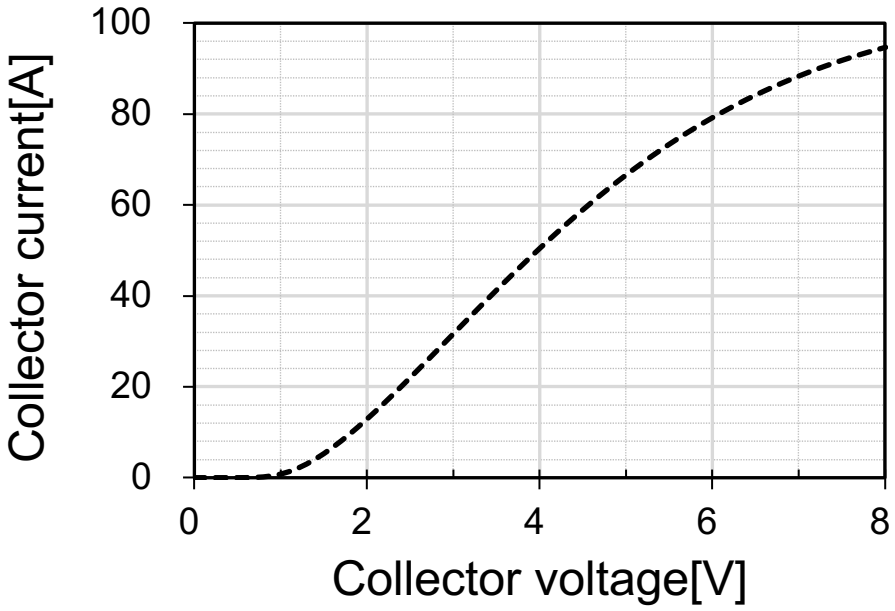


Fig. 5.6 Collector-Emitter current versus voltage by TCAD simulation.

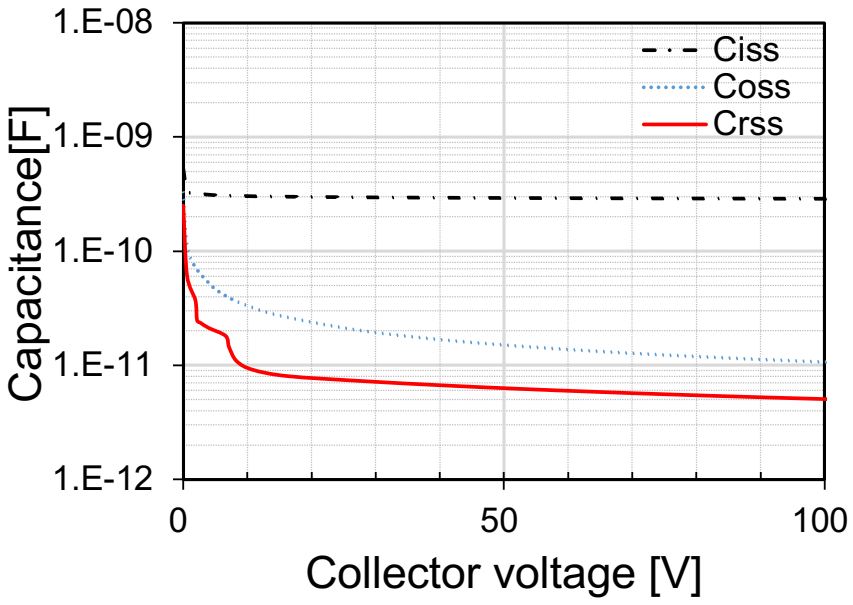
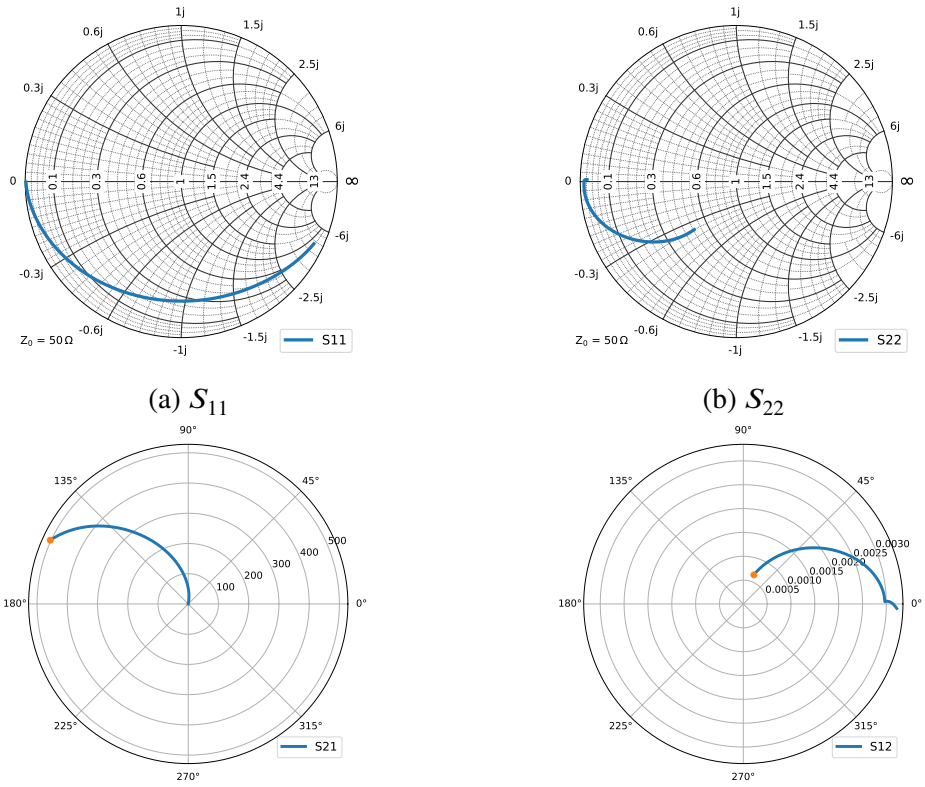


Fig. 5.7 Collector voltage dependences of the input, output, and feedback capacitances calculated using TCAD simulation.

Table 5.2 Device parameters of the TCAD device model

L_{drift}	130 μm	L_{trench}	4 μm
$L_{\text{n+}}$	1.3 μm	$L_{\text{p+}}$	5 μm
W_{trench}	2 μm	$L_{\text{p-base}}$	3.5 μm
$n_{\text{p-base}}$	5×10^{16} cm^{-3}	n_{ndrift}	1×10^{14} cm^{-3}
$n_{\text{n-buffer}}$	2×10^{17} cm^{-3}	$L_{\text{n-buffer}}$	2 μm

The S-parameters of assumed simulation model structure can be calculated using the small-signal ac analysis function of a TCAD simulator. Table 5.3 presents the frequency dependence of the S-parameters. Fig. 5.8 shows the S-parameters plotted on the Smith charts, which are representation in the reflection coefficient plane. In the graphs of S_{11} and S_{22}, the abscissa is the magnitude of the real part of the reflection coefficient. The upper half has a positive complex component and the lower half has a negative complex component. It is normalized by the characteristic impedance. The reflection coefficient is 0 at the center, 1 at the right end, and -1 at the left end, respectively. In the graphs of S_{12} and S_{21}, the radial direction indicates the magnitude of the reflection coefficient, and the angular direction indicates the phase. Here, the S-parameters were computed from 100 kHz to 1 GHz.



(a) S_{11} (b) S_{22}

(c) S_{21} (d) S_{12}

Fig. 5.8 Smith charts of the calculated S-parameter when $V_d = 100$ V.

5.3 Analysis of device operation during the oscillation

In this section, stability analysis is carried out using the oscillation conditional factor $\alpha(\omega)$ introduced in chapter 3. The collector voltage dependence of the critical gate resistance to suppress the oscillation is calculated and compared with the experimental results.

A small-signal equivalent circuit is introduced to analyze the oscillation condition. High-side diode D_1 and L_m can be considered to be shorted during SC type II. The gate voltage source V_{Drive} can be replaced as its source impedance Z_{s} and small-signal source V_{s}. Based on these assumptions, C_{DC} can ignore its impedance in the frequency range where oscillation phenomena occur. The chopper circuit presented in Fig. 5.1 can be transformed into an equivalent small-signal circuit, as shown in Fig. 5.9. Z_{L} is defined as $Z_{\mathrm{L}} = j\omega L_{\mathrm{DC}}$. $\hat{S}$ is defined as the S-parameter in the area enclosed by the dotted black line in Fig. 5.9.

Table 5.3 S-parameter calculated by TCAD simulator

Freqency Hz	S_{11} MAG. ANG.	S_{21} MAG. ANG.	S_{12} MAG. ANG.	S_{22} MAG. ANG.
0.10 M	0.928 -24.99	0.0006 68.51	479.9 152.0	0.4826 -141.3
0.50 M	0.778 -79.74	0.0016 41.17	216.9 117.9	0.8658 -161.5
1.00 M	0.806 -112.6	0.0021 28.72	125.0 103.3	0.9456 -169.2
5.00 M	0.955 -161.7	0.0026 8.222	22.50 81.48	0.9803 -177.9
10.0 M	0.979 -170.3	0.0027 4.288	10.05 78.54	0.9803 -179.0
50.0 M	0.994 -177.9	0.0027 1.400	1.573 77.67	0.9811 -179.8
100 M	0.996 -178.9	0.0027 1.561	0.705 78.30	0.9811 180.0
500 M	0.997 -179.8	0.0028 3.415	0.127 82.43	0.9753 179.5
1.00 G	0.997 -179.9	0.0030 3.401	0.073 76.549	0.9677 179.5

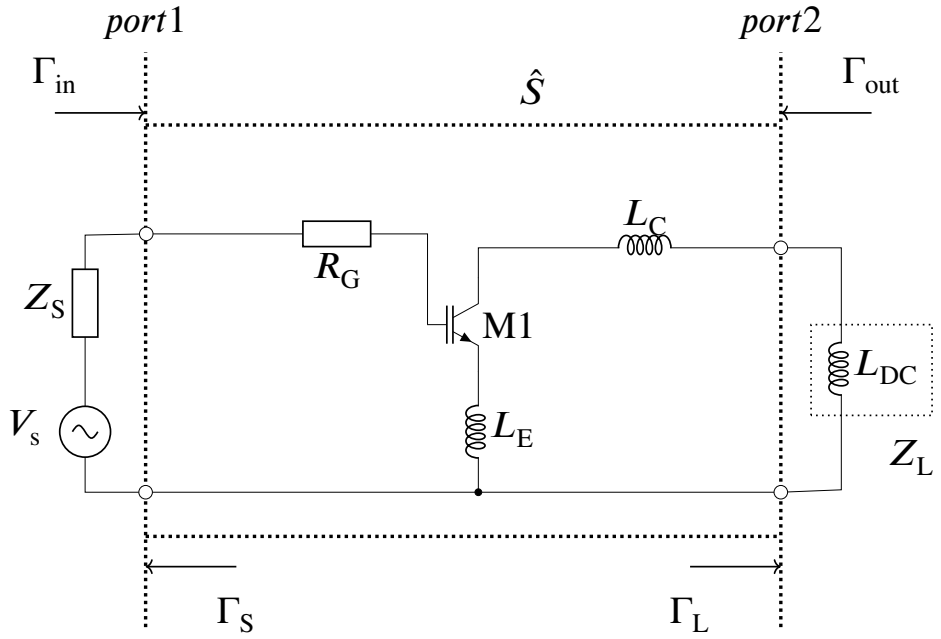


Fig. 5.9 Simplified equivalent circuit.

Fig. 5.10 shows the signal flow graph of the equivalent circuit shown in Fig. 5.9. b_s is the input signal. a_1, b_1, a_2, and b_2 are the power waves defined as in eq. (3.1) and eq. (3.2).

Γ_L and Γ_S are the input and load reflection coefficient, respectively. These are defined as in eq. (3.11) and written as

$$\Gamma_L = \frac{Z_L - Z_0}{Z_L + Z_0}, \Gamma_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \tag{5.1}$$

where Z_S and Z_L are the impedances of the signal source and the load, respectively. Their impedances are expressed as $Z_S = i\omega L_G$ and $Z_L = i\omega L_{DC}$, respectively.

Using the signal flow graph analysis technique [84, 85], Γ_{in} can be written as:

$$\Gamma_{\mathrm{in}} = \frac{b_1}{a_1} = S_{11} + \frac{S_{12}S_{21}\Gamma_{\mathrm{L}}}{1 - S_{22}\Gamma_{\mathrm{L}}}. \tag{5.2}$$

The transfer function b_1/b_{s} can be written as follows [84, 85]:

$$\frac{b_1}{b_{\mathrm{s}}} = \frac{\Gamma_{\mathrm{in}}}{1 - \Gamma_{\mathrm{S}}\Gamma_{\mathrm{in}}}. \tag{5.3}$$

The oscillation condition can be calculated using the loop gain of the signal flow graph is shown in figure 5.10. The oscillation condition factor $\alpha(\omega)$ is written as:

$$\alpha(\omega) = -\left(S_{11} + \frac{S_{12}S_{21}\Gamma_{\mathrm{L}}}{1 - S_{22}\Gamma_{\mathrm{L}}}\right)\Gamma_{\mathrm{S}}. \tag{5.4}$$

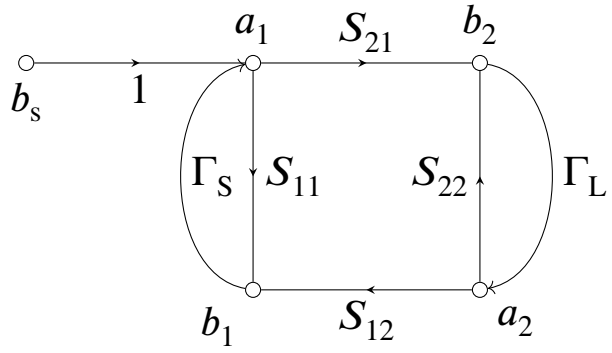


Fig. 5.10 Equivalent signal flow graph.

The dependence of the critical gate resistance on the collector voltage to suppress the oscillation is calculated using the oscillation condition factor $\alpha(\omega)$ and compared with the experimental results. Figure 5.11 shows the gate-resistance dependence of the Nyquist plot of $\alpha(\omega)$. The S-parameter of the IGBT is calculated at $\mathrm{V_c}$ = 100 V and $\mathrm{V_g}$ = 15 V using the TCAD simulation. As the resistance increases from 0.0 Ω to 10 Ω, the intersection of the plotted line and the imaginary axis moves from left to right of (-1, 0j). The intersection represents the loop gain intensity. Thus, the oscillation is suppressed when the intersection is to the right of $(-1, 0j)$.

Figure 5.12 shows the calculated collector-voltage dependence of the gate resistance to suppress oscillations. The gate resistance decreases as the collector voltage decreases. These results are consistent with the experimental results.

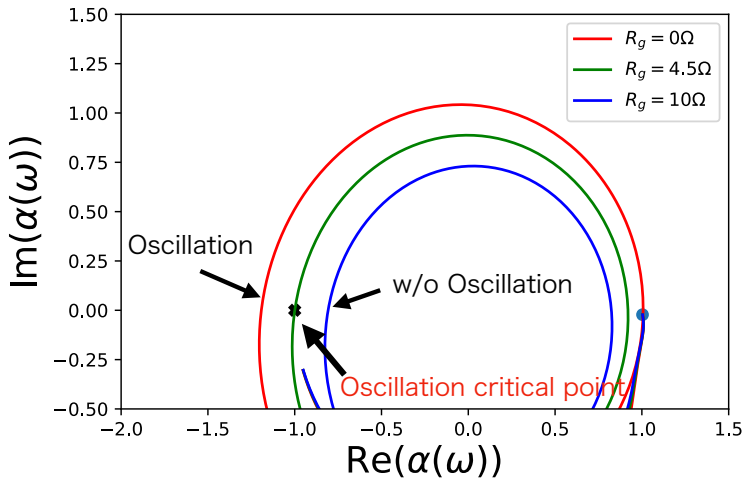


Fig. 5.11 The Nyquist plot of the oscillation condition factors α(ω) when V_c=100 V and V_g = 20 V.

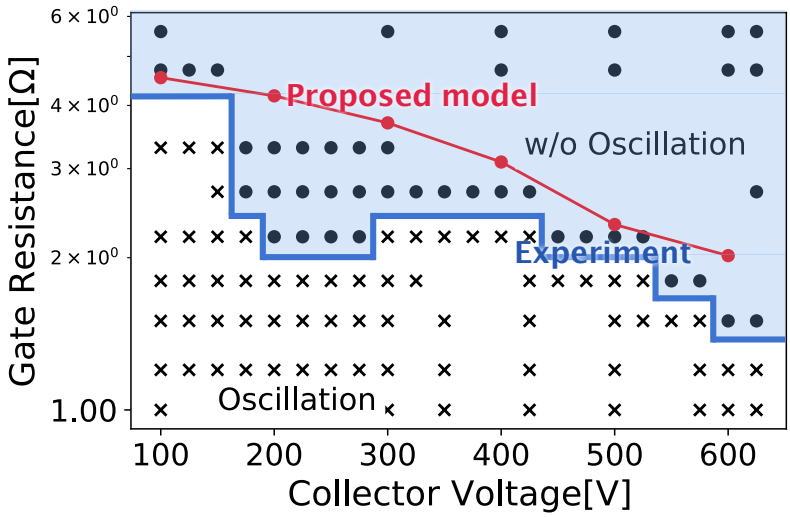


Fig. 5.12 Calculated drain voltage dependence of the gate resistance to suppress the oscillation.

5.4 Analysis of oscillation mechanism

The origin of the oscillation suppression during SC type II at higher collector voltages is discussed in this section.

Figures 5.14 and 5.13 show the electric field and carrier distribution during SC type II calculated using the TCAD simulation when V_c = 100 V and 600 V, respectively. In Fig. 5.14, the solid and dotted lines indicate the electron and hole distributions, respectively. The cut-out position is the right end of the cross-sectional view of the device shown in Fig. 5.5. The conductivity modulation is induced by the hole injection from the collector side.

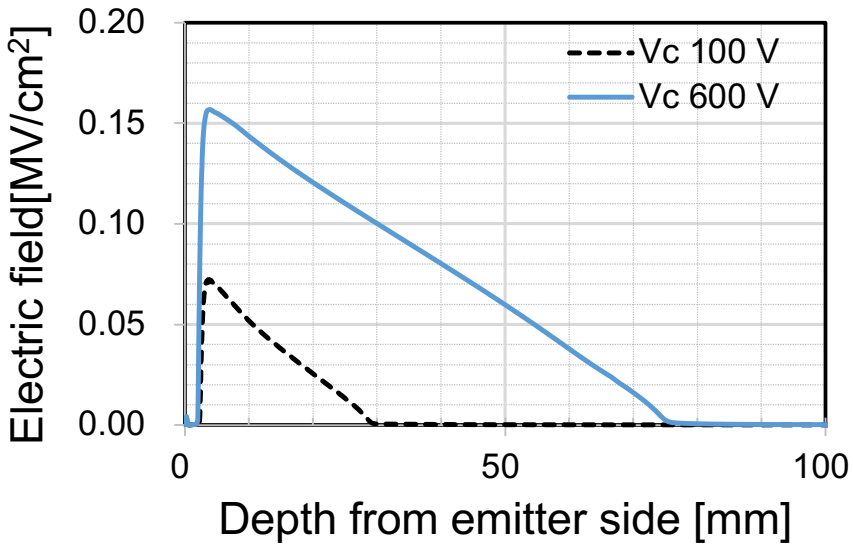


Fig. 5.13 Electric field distribution during SC type II when V_c = 100 V and 600 V.

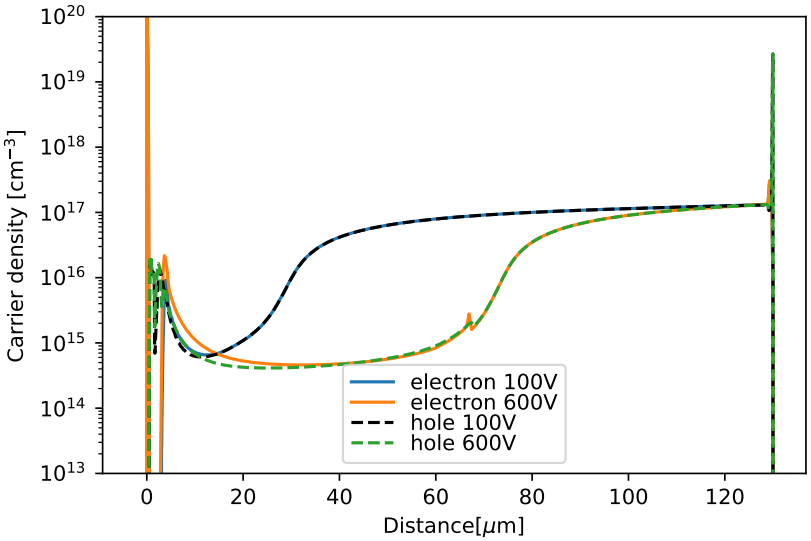


Fig. 5.14 Carrier density distribution during SC type II when V_c = 100 V and 600 V.

When V_c is 100 V, there is a region where the carrier density decreases up to approximately 30 μm from the junction surface. This carrier distribution indicates that the electron-hole plasma from the device surface to 30 μm is swept out when V_c = 100 V. As observed in the electric field distribution in Fig. 5.13, the electric field increases and exhibits a triangular shape in this region. The region with high electric field intensity increases to 70 μm by increasing the collector voltage up to 600 V, as shown in Fig. 5.14. The maximum electric field is not higher than the critical electric field of silicon. Therefore, it is considered that this oscillation is not caused by the carrier generation mechanism of impact ionization, as in the IMPATT oscillation.

Figure 5.15 also shows the current density distribution during SC type II using the TCAD simulation when V_c = 100 V and 600 V. The current flows from the collector side through the floating p-region and trench channel to the emitter. A narrowing of the current occurs in the high-electric-field region, and its width becomes narrower as the collector voltage increases.

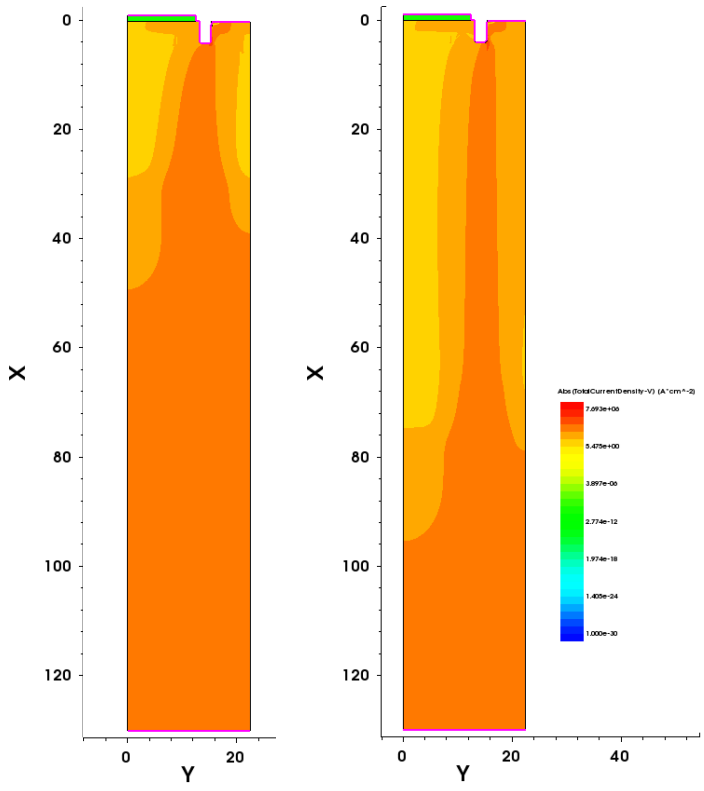


Fig. 5.15 Current density distribution when V_c = 100 V and 600 V.

In the TCAD simulator, ξ_{total} is expressed using dc and ac components [78]. The ac response ξ to the external field is defined as follows:

$$\xi_{\text{total}} = \xi_{\text{DC}} + \xi_{\text{AC}} = \xi_{\text{DC}} + \xi e^{i\omega t}. \tag{5.5}$$

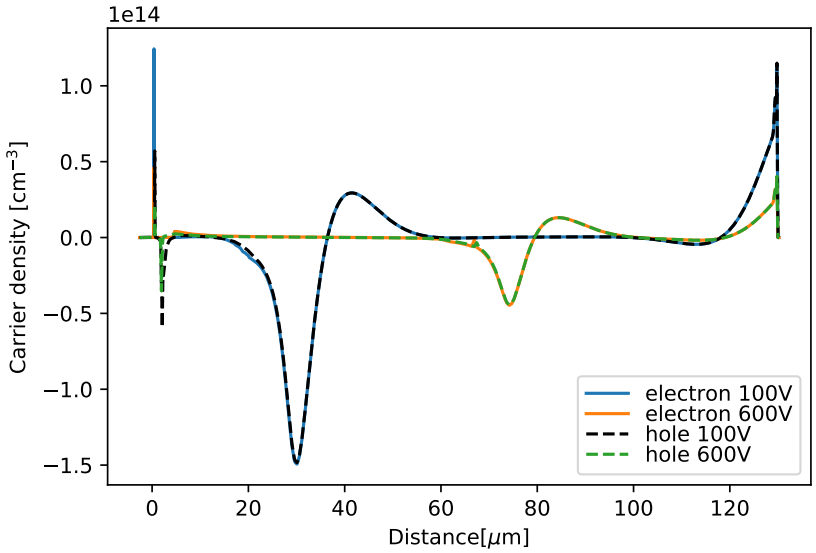


Fig. 5.16 Response Distribution at 10MHz.

Figure 5.16 shows the real and imaginary parts of the frequency responses of the electrons and hole densities against the collector voltage. The cases of 100 V and 600 V collector voltages are shown. The carrier density response at the plasma region boundary increases under each voltage condition. This carrier density response at 100 V is higher than that at 600 V. These results imply that in the oscillation state, increase or decrease in the thickness of the high-electric-field region is propagated as a modulation of the carrier concentration at the edge of the electron−hole plasma region.

Figure 5.17 shows the electric potential response inside the device when V_c is 100 V and 600 V. This result shows that the change in the electric potential corresponds to the carrier swept region and it depends on the collector voltage. Figure 5.18 shows the derivative of the electric potential response. This can be considered as the response of the electric field.

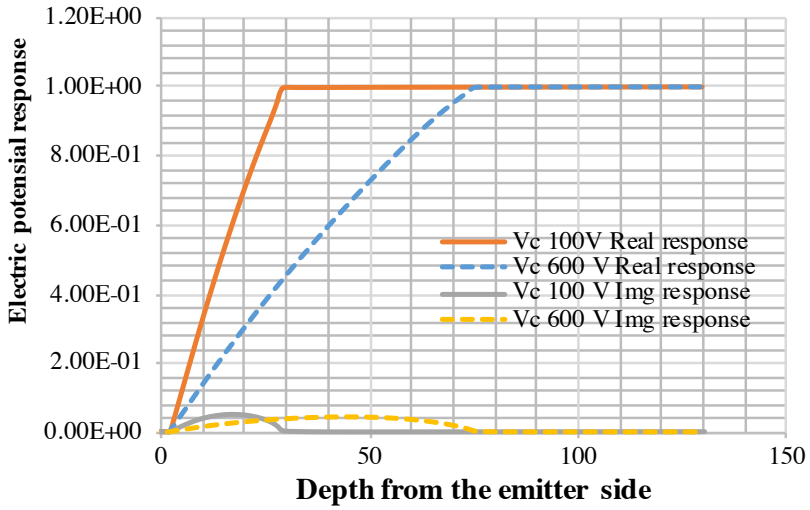


Fig. 5.17 The distributions of electric potential responses for corrector voltages when V_c = 100 V and 600 V.

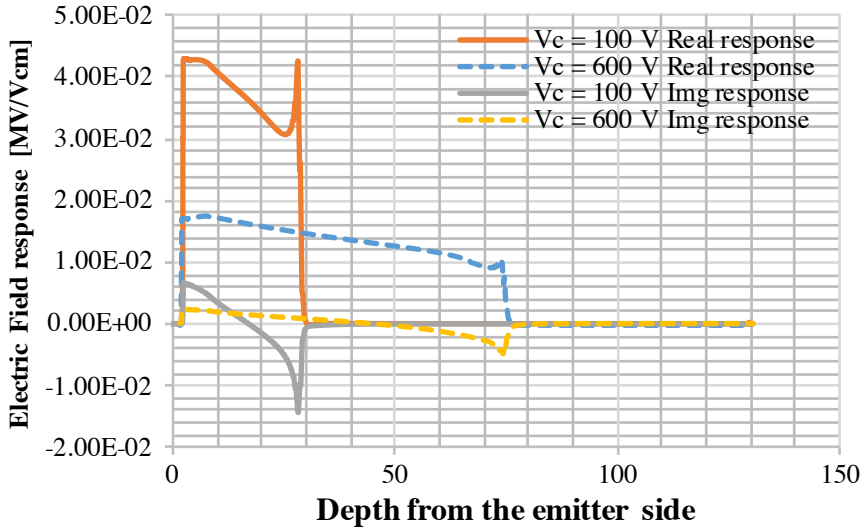


Fig. 5.18 Electric field responses for corrector voltages calculated by derivation of the potential response when V_c = 100 V and 600 V.

Figure 5.19 and 5.20 shows the time dependence of the electric field calculated by real and imaginary parts of the electric field response shown in Fig. 5.18. When the collector voltage is 100 V, the response of the electric field is quadrangular rather than triangular. The width of the high-electric-field region decreases when the collector voltage is 100 V than when the collector voltage is 600 V. When the collector voltage is 600 V, the electric field response remains small because of the wider high electric field region.

These periodic modulations of electron−hole plasma density and electric field intensity have been reported in previous studies using TCAD mixed-mode simulations [74, 86]. The proposed method can consider the internal device behavior without using mixed-mode simulation.

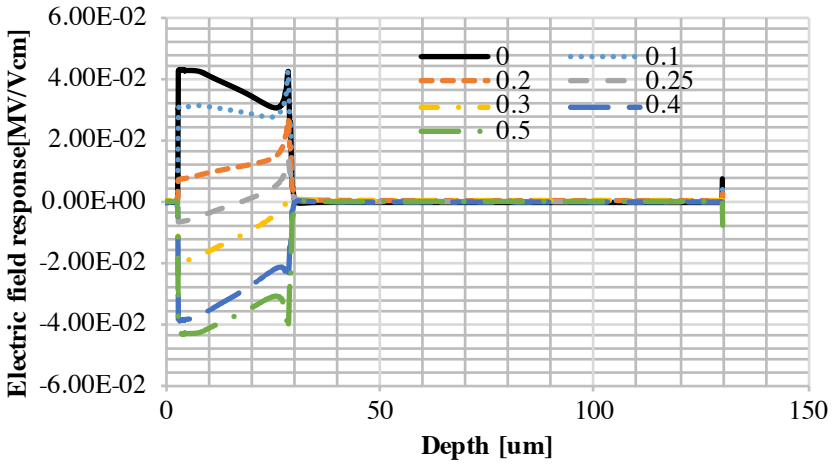


Fig. 5.19 The time dependences of electric field distribution when $V_c = 100$ V.

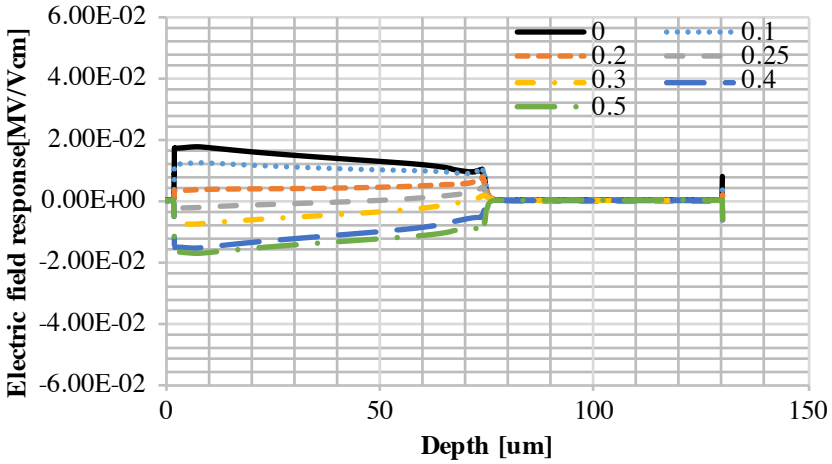


Fig. 5.20 The time dependences of electric field distribution when $V_c = 600$ V.

As mentioned above, the electron-hole plasma contributes to the oscillation in response to the external field. The carrier density and electric field distribution response to the external field are reduced when a higher voltage is applied. In the oscillation state, the current response to the external field depends on the carrier density, electric field, and carrier mobility.

These properties depend on the position in the device and interact with each other. Hence estimating the current response is generally complicated. However, the TCAD simulation can simultaneously calculate these effects as a Y-parameter.

Figure 5.21 and figure 5.22 show the frequency dependence of the Y-parameter from collector to collector and collector to gate when $V_c = 100$ V and $V_c = 600$ V, respectively. As can be seen from these results, the frequency response at lower voltages is greater than that at higher voltages.

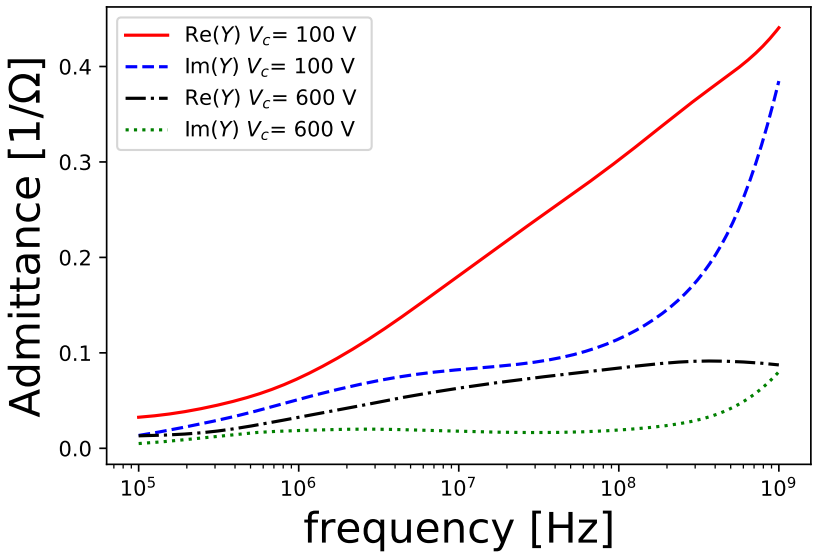


Fig. 5.21 Frequency dependences for Y_{cc} when $V_c = 100$ V and 600 V.

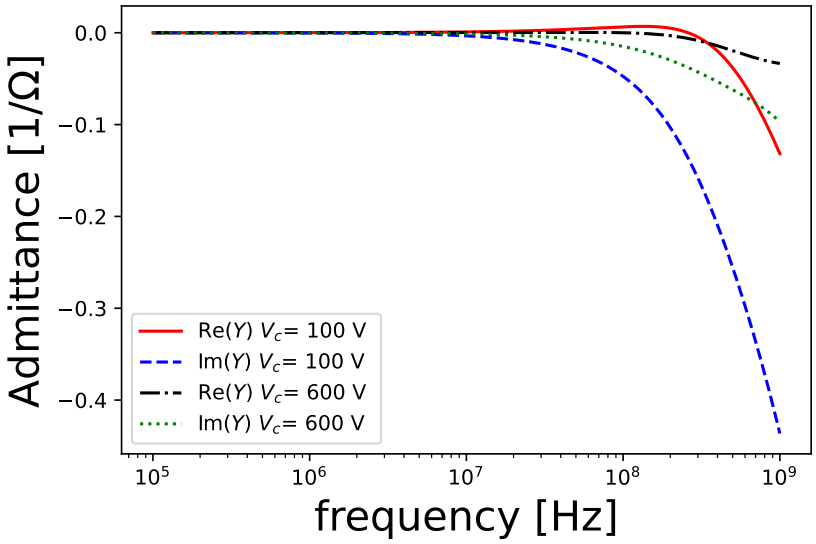


Fig. 5.22 Frequency dependences of Y_{gc} when $V_c = 100$ V and 600 V.

5.5 Summary

The oscillation phenomenon of trench-type IGBTs during SC type II was experimentally investigated. The oscillation during SC operation could be suppressed by increasing the gate resistance. The resistance required for oscillation suppression decreased with the increase in the collector voltage. The oscillation conditions were calculated from the signal flow graph using the S-parameter of the trench-type IGBT based on the TCAD simulation. The calculation results reproduced the locus of the collector voltage dependence of the gate resistance required to suppress oscillation. The proposed method can be used to evaluate the oscillation condition depending on the collector voltage and gate resistance through a simple calculation using a signal flow method and the S-parameters, computed using a TCAD device simulation.

The internal state of the device during the oscillation was also investigated using a TCAD simulation. It has been found that a high-electric-field region is formed at the base-drift layer boundary, and the effect of the carrier density modulation is transmitted to the collector side through the electron-hole plasma region during the oscillation. Moreover, the carrier and current responses to the external field are higher at lower collector voltages than these at higher collector voltages. The volume of high-electric-field was smaller than that at high collector voltages. On the other hand, the volume of electron-hole plasma region is lager at lower collector voltages than that at higher collector voltages. These results suggest that the transfer characteristics of the carrier distribution through the carrier discharge region and the electron-hole plasma causes the drain voltage dependence of the short-circuit oscillation conditions.

Chapter 6

Conclusions

6.1 Summary

Power devices are expected to play an important role in the effort to achieve net zero CO_2 emissions. In this dissertation, the novel design method to analyze the stable operation of power devices is proposed. This method is based on the S-parameter obtained from TCAD, and the internal operating state of the device can be directly incorporated into the stability analysis. The proposed method is applied to the oscillation phenomena of SiC-MOSFETs and Si-IGBTs during short-circuit operation, and the effectiveness of the method is verified by comparing the calculation results of the proposed method with those of conventional calculation methods and experimental results.

In chapter 1, the trend of research and development on improving the characteristics of Si-IGBTs and SiC-MOSFETs for volume and weight reduction and efficiency improvement of power conversion systems are described.

In chapter 2, the oscillation phenomena of Si-IGBTs and SiC-MOSFETs in power conversion systems is discussed, and previous studies on the suppression of oscillation phenomena are summarized. The requirement of the comprehensive approach for power device design and power conversion system design to take advantage of the improvement of power devices is discussed.

In chapter 3, the novel method for analyzing circuit stability based on the S-parameter and the SFG is proposed. This method allows us to calculate the stability of the entire circuit system by considering the external field response without simplifying the internal device states such as carrier and electric field distribution in the device.

By applying Mason's rule to the SFG, the signal gain for the focused mode can be easily calculated. In addition, stability analysis using the Nyquist plot allows the designer to not only judge the stability of the design parameters but also to quantify the the margins.

In chapter 4, the usefulness of the proposed method is verified by applying it to the oscillation phenomena of SiC MOSFETs during SC Type II operation. The S-parameters are calculated using TCAD for a commercial SiC MOSFET, and stability analysis is carried out. The critical gate resistance for oscillation suppression is obtained by the mixed mode TCAD simulation and proposed method. The agreement between the proposed method and the results of TCAD mixed mode simulation is confirmed. In this study, stability analysis is carried out for the two modes that are the oscillation caused by coupling with parasitic elements of the circuit and oscillation induced by devices connected in parallel. The characteristics of each mode during short-circuit operation are clarified, and the stability phase diagrams in the design parameters space are calculated for each oscillation mode.

In chapter 5, the proposed method is applied to the oscillation phenomena of Si-IGBTs under SC Type II. It was experimentally confirmed that oscillation occurred during SC Type II and it was suppressed by increasing the gate resistance and the collector voltage. The stability analysis using the proposed method is carried out. Using the Nyquist plot, the critical gate resistance required to suppress the oscillation is obtained and its the collector voltage dependence is estimated. As a result, it is confirmed that the critical gate resistance decreases as the collector voltage increases. Then the proposed method agrees well with the experimental results. The internal behavior of the device in the oscillation state is also analyzed. During the short-circuit operation, the high electric field region with the triangular electric field distribution is formed at the boundary between the base and drift layers due to decrease in the carrier density. When this region expands or contracts due to the external field, the carrier distribution at both ends of the electron-hole plasma region is modulated. This modulation is found to be more responsive when the collector voltage is lower. From the correspondence with the experimental results, it can be considered that the response to the external field of the high field region and the plasma region caused by the short circuit, in combination with the external circuit, causes the oscillation during the short circuit.

6.2 Significance of the proposed method to the power converter design and future development

In chapters 3 to 5, the novel method for the stability analysis of power semiconductor devices has been proposed. In the conventional TCAD simulation, device structure optimization at the design stage for different operating conditions in various application fields could not be performed in realistic calculation time. The proposed method enables seamless multilevel

analysis from the microscopic internal state of the device to the entire power conversion system.

Although the analysis focused on the short-circuit operation in this study, the proposed method can be applied to any device operating state. Since the proposed method analyzes the stability of equivalent circuits in the focused operating state, it is important to consider what kind of equivalent circuits is prepared. The simplest approach is to perform a stability analysis for the voltage and current conditions of the entire safety operation area (SOA). It is easy to evaluate the validity of the device design and determine the recommended operating condition from this analysis. Although it is the simple and effective method using the SOA as the scope of the evaluation, it is more important to conduct the analysis assuming actual system operating conditions. Estimating the noise effects and lifetime of power devices based on the realistic operating condition of the system has become an important research issue. In recent years, many studies on the system design from mission profiles have been reported [87, 88]. Similar to these reports, the proposed method can be applied to the stability analysis in operating conditions determined based on the mission profile of the system.

The state to be analyzed can also be determined by other simulations. A study applying the proposed method in this dissertation to the stability analysis of switching transient states has been reported [89]. In this report, the transient states to be calculated are determined by SPICE simulation, and the stability of each time step is analyzed.

It is important to reflect the temperature of the device in the considering circuit stability. Temperature change affects the circuit stability because of the change in the threshold voltage and the amplification factor of the MOSFET. Temperature effects can be treated by calculating S-parameters using the results of TCAD device simulations under the focused temperature conditions.

A remaining research challenge is to determine the optimal device and circuit parameters based on the trade-off between loss and stability through stability analysis of the device operation within realistic power modules and application circuits.

In this study, the parameters of the circuit network are determined from actual impedance measurements, whereas the S-parameter can be calculated using electromagnetic (EM) simulation. Therefore, stability analysis can be performed in combination with highly-precision models of modules, packages, and circuits obtained by the EM simulation. We can not only optimize device parameters but also optimize external circuits design calculating S-parameters for each design parameter of modules, packages, and circuits by the EM simulations. It is also possible to optimize the design parameters of both the devices and modules simultaneously.

One of the advantages of the proposed method is that it allows to selectively analyze the stability of the target states. In the optimal design parameter search, it is necessary to repeatedly calculate the stability for multiple operating conditions for each set of search parameters. The proposed method enables efficient calculation because the stability can be computed in short time for each parameter search steps. Therefore, the proposed method can be used together with machine learning and deep learning methods, which will become mainstream in the future, to achieve more advanced design optimization.

Then, the proposed method can be a powerful tool for enabling the overall optimization design of power conversion systems.

This dissertation proposes the design method to calculate the stability of the power circuit consisting of power switching devices and passive and parasitic circuit components. The results are expected to contribute to the expansion of power electronics by maximizing the potential of power devices that have not been fully utilized and by improving the efficiency of power electronic system development.

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Appendix A

Matrix calculation

Two port matrix

For the calculation of the S-parameter when a small-signal equivalent circuit is given, the ABCD matrix can be used to perform a simple matrix calculation.

The ABCD matrix is defined as

$$\begin{pmatrix} v_1 \\ i_1 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_2 \\ i_2 \end{pmatrix}, \tag{A.1}$$

where v_i and i_i are defined as Fig. 3.3.

When there is an impedance component Z in series with the two-terminal network as shown in Figure A.1, ABCD matrix is written as

$$\hat{F} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} 1 & Z \\ 0 & 1 \end{pmatrix}. \tag{A.2}$$

When there is an impedance component Z is connected in the two-terminal network as shown in Figure A.2, ABCD matrix is written as

$$\hat{F} = \begin{pmatrix} 1 & 0 \\ 1/Z & 1 \end{pmatrix}. \tag{A.3}$$

Considering the small signal FET is written in Figure A.3, ABCD matrix is written as

$$\hat{F} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} = \begin{pmatrix} -\frac{1}{g_m r_0} & -\frac{1}{g_m} \\ 0 & 0 \end{pmatrix}, \tag{A.4}$$

where g_m is a transfer conductance and r_0 is output resistance.

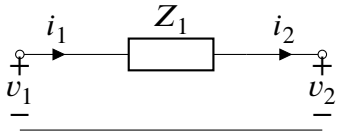

Fig. A.1 A two-port network consisting of a series impedance Z_1

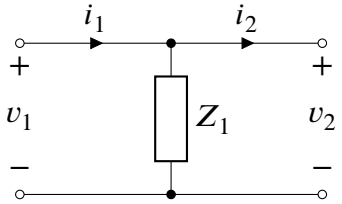

Fig. A.2 A two-port network consisting of a shunt impedance Z_1

Fig. A.3 A small signal model of a FET.

RESEARCH HISTORY

Publication

1. Hiroshi Kono and Ichiro Omura, ”Study of parasitic oscillation of a multi-chip SiC MOSFET circuit based on a signal flow graph model by TCAD simulation”, Solid-State Electronics, 177, art. no. 107884, (2021).

2. Hiroshi Kono and Ichiro Omura, ”Parasitic Oscillation Analysis of Trench IGBT During Short-Circuit Type II Using TCAD-Based Signal Flow Graph Model”, IEEE Transactions on Electron Devices, vol. 69, no. 10, pp. 5705-5712, (2022).

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1. Hiroshi Kono and Ichiro Omura, ”Study of parasitic oscillations in trench IGBT during short-circuit type II based on signal flow graph model”, Proceedings of 12th International Conference on Integrated Power Electronics Systems (CIPS2022), pp.487-492, (2022).

Related Papers

1. H. Kono, T. Suzuki, M. Mizukami, C. Ota, S. Harada, J. Senzaki, K. Fukuda, T. Shinohe, ”1360 V, 5.0 mΩcm2 double-implanted MOSFETs fabricated on 4H-SiC(000-1)”, Materials Science Forum, 645-648, pp. 987-990, (2010).

2. H. Kono, T. Suzuki, K. Takao, M. Furukawa, M. Mizukami, C. Ota, C., S. Harada, J. Senzaki, K. Fukuda, T. Shinohe, ”1.4kV double-implanted MOSFETs fabricated on 4H-SiC(000-1)”, Materials Science Forum, 679-680, pp. 607-612, (2011).

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9. H. Kono, T. Iguchi, T. Hayakawa, H. Irifune, T. Kawano, M. Furukawa, K. Sano, M. Yamaguchi, H. Suzuki, G. Tchouangue, ”3.3kV All SiC MOSFET Module with Schottky Barrier Diode Embedded SiC MOSFET”, PCIM Europe digital days 2021; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, pp. 1-6, (2021).