IEICE Electronics Express, Vol.3, No.13, 287–291

On-chip solar battery structure for CMOS LSI

Yutaka ARIMA[a)] **and Masaya EHARA**

Center for Microelectronic System, Kyushu Institute of Technology

680–4, Kawazu, Iizuka, Fukuoka 820–8502, Japan

a) *arima@cms.kyutech.ac.jp*

Abstract: A built-in method of on-chip solar battery in a CMOS LSI is proposed. The proposed solar battery can be formed using conventional CMOS process technology. It can generate a high voltage of 0.6–0.83 V by a series connection structure of two types of p-n junction diodes formed with the CMOS circuit simultaneously on the LSI chip. The generated voltage is sufficient to drive the conventional CMOS circuit without modification. The test chip was produced experimentally using conventional 0.35 μm CMOS technology, and the drive performance of the on-chip solar battery was evaluated. The conversion efficiency of the proposed solar battery was 2.6%. The area of the solar battery required for power consumption was 6.1 $mm^2/\mu W$ in the case of the 2000lx illumination.

Keywords: solar battery, on-chip, CMOS, self-powered system

Classification: Integrated circuits

References

[1] M. Miyazaki, H. Tanaka, G. Ono, T. Nagano, N. Ohkubo, and T. Kawahara, "Electric-Energy Generation through Variable-Capacitive Resonator for Power-Free LSI," *IEICE Trans. Electron.*, vol. E87-C, no. 4, pp. 549–555, April 2004.

[2] Y. Yoshida, F. Utsunomiya, and T. Douseki, "Sub-1-V Power-Supply System with Variable-Stage SC-Type DC-DC Converter Scheme for Ambient Energy Sources," *IEICE Trans. Electron.*, vol. E88-C, no. 4 pp. 484–489, April 2005.

[3] J. Nanjo, K. A. H. Mostafa, K. Takada, Y. Kobayashi, T. Miyazaki, and S. Nomura, "Si MIS Solar Cells by Anodization," *IEICE Trans. Electron.*, vol. E76-C, no. 1, pp. 136–141, Jan. 1993.

[4] T. Douseki, M. Yonemaru, E. Ikuta, A. Matsuzawa, A. Kameyama, S. Baba, and T. Mogami, "Ultra low-Voltage MTCMOS/SOI Circuits for Battery less Mobile System," *IEICE Trans. Electron.*, vol. E87-C, no. 4, pp. 437–447, April 2004.

[5] K. Itoh, A. R. Fridi, A. Bellaouar, and M. I. Elmasry, "A Deep Sub-V, Single Power-Supply SRAM cell with Multi-Vt, Boosted Storage node and Dynamic Load," *1996 Symp. VLSI.*

DOI: 10.1587/elex.3.287
Received May 16, 2006
Accepted June 05, 2006
Published July 10, 2006

IEICE Electronics Express, Vol.3, No.13, 287–291

1 Introduction

A self-powered system is effective for applications that do not limit the utilization place as a ubiquitous network system. Some LSI technologies such as batteryless chips or on-chip batteries have been researched to realize such a self-powered system. Self-powered systems that utilize ambient energy such as vibrations or differences in temperature have been reported [1, 2]. However, they have problems such as equipment size and the stability of their energy source. The solar battery, which has light as an energy source, can be made with a silicon semiconductor and is promising as an on-chip battery. However, the generated voltage of conventional semiconductor solar batteries is approximately 0.3–0.4 V [3].

A conventional CMOS circuit cannot be driven with such a low supply voltage. Some modified CMOS circuits that can operate with such a low supply voltage have been proposed [4, 5]. However, the circuits have to use multithreshold value MOSFETs, and circuit configuration must be modified, and they have the disadvantage of high design and manufacturing costs. Therefore, the development of an on-chip solar battery that can be generated with sufficient voltage to drive a conventional CMOS circuit is required. The on-chip solar battery should be formed simultaneously with the CMOS circuit using conventional CMOS technology to reduce the manufacturing cost.

2 Structure of on-chip solar battery and test chip

Figure 1 shows the structure of the on-chip solar battery. The equivalent circuit configuration (a) and section structure (b) of the device are shown. By the series connection of two types of photodiode that can be formed during the source drain process in conventional CMOS technology, the solar battery can be generated with double voltage. The two types of photodiode are a p-n junction diode consisting of a N-well and a P+ source drain (S/D) and a diode consisting of a P-sub and a N+S/D. These photodiodes are formed simultaneously with the source drain of the pMOSFET and nMOSFET. Therefore, they can be formed by expanding a source part of each MOSFET. The two photodiodes are connected in series by electrically short-circuiting with a N-well node and a P-sub node. Because the substrate potential of each MOSFET rises as a result of the circuit configuration, the threshold value of each MOSFET decreases. The change in the threshold value of the MOSFETs increases the supply voltage margin, and static leakage current increases. The CMOS circuit is covered by a shading layer utilizing a metal layer.

Figure 2 shows a micrograph of the test chip. The test chip was produced by 0.35 μm, 1-poly, 3-metal, standard CMOS process. The CMOS circuit for the drive experiment uses a full adder as a combinational circuit and a 7-bit counter as a sequential circuit with a typical circuit configuration. The full adder consists of 34 MOSFETs (L=0.35 μm, Wn=0.7 μm, Wp=2.1 μm). The circuit area of the full adder is 320 μm^2. The 7-bit counter consists of 274 MOSFETs (L=0.35 μm, Wn=Wp=3.0 μm). The circuit area of the 7-bit counter is 4500 μm^2. Two types of photodiode of equal size were formed.

DOI: 10.1587/elex.3.287
Received May 16, 2006
Accepted June 05, 2006
Published July 10, 2006

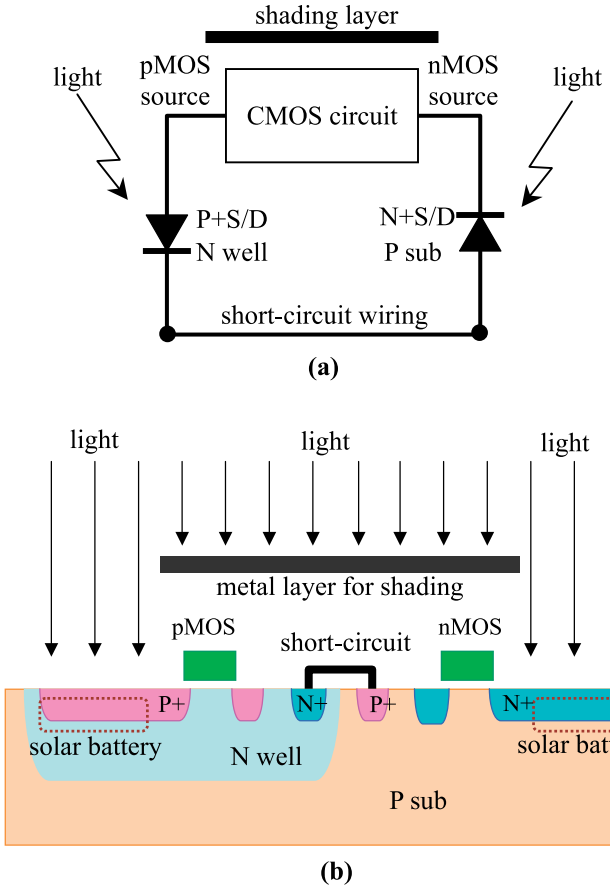


Fig. 1. Structure of on-chip solar battery: (a) equivalent circuit structure (b) section structure of device

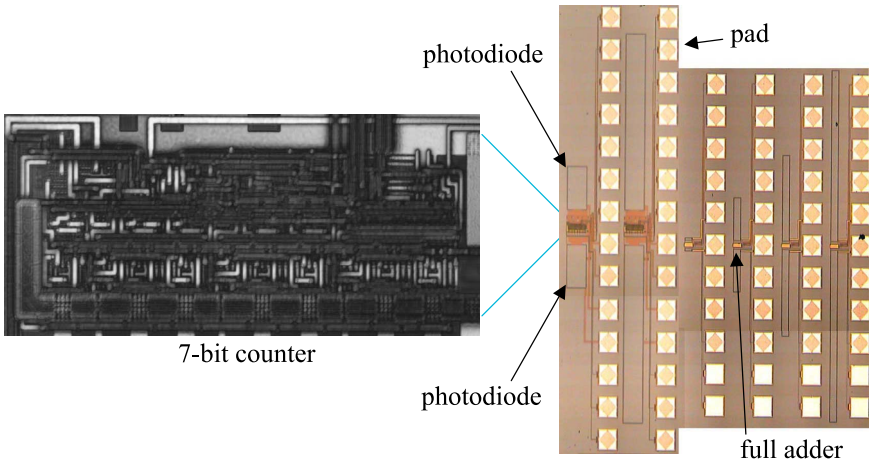


Fig. 2. Micrograph of test chip

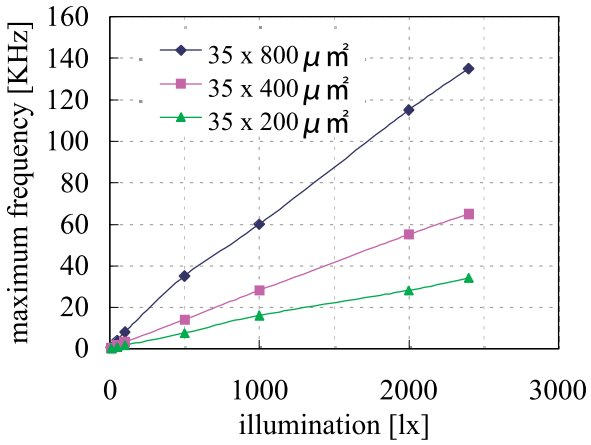
There are five sizes of photodiode in the test chip: they are $100\times200\,\mu m^2$, $100\times800\,\mu m^2$, $35\times200\,\mu m^2$, $35\times400\,\mu m^2$, and $35\times800\,\mu m^2$.

3 Experimental results

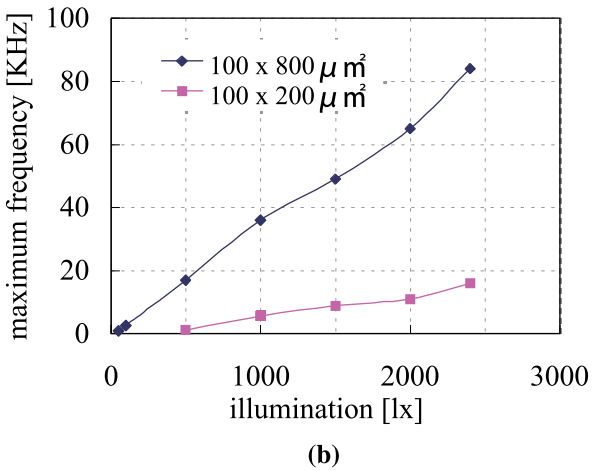
Figure 3 shows some evaluation results of the test chip. (a) and (b) show the maximum operating frequencies corresponding to illuminations for the

DOI: 10.1587/elex.3.287
Received May 16, 2006
Accepted June 05, 2006
Published July 10, 2006

full adder and the 7-bit counter driven with the proposed solar battery. The color temperature of the light is 5500 K. Each maximum operating frequency is in proportion to the illumination and size of the photodiode. Because power consumption of the 7-bit counter is larger than that of the full adder, the maximum operating frequency of the 7-bit counter is comparatively low. The scale of the CMOS circuit that can be driven with the solar battery is determined by the generating capacity of the solar battery and the power consumption of the circuitry. (c) shows the I-V characteristic of the proposed solar battery in the case of different illumination conditions. Each size photodiode is $200\times500\,\mu m^2$. The open voltage Vco of the proposed solar battery is 0.6–0.83 V, and the maximum conversion efficiency is 2.6%. The area of solar battery required for the power consumption of the CMOS circuit was $6.1\,mm^2/\mu W$ in the case of the 2000lx illumination. This corresponds to the outdoor environment on a cloudy day. In the bright environment of illumination 10000lx, the necessary area of the solar battery becomes $1.15\,mm^2/\mu W$. The conversion efficiency can be improved by changing the passivation materials.

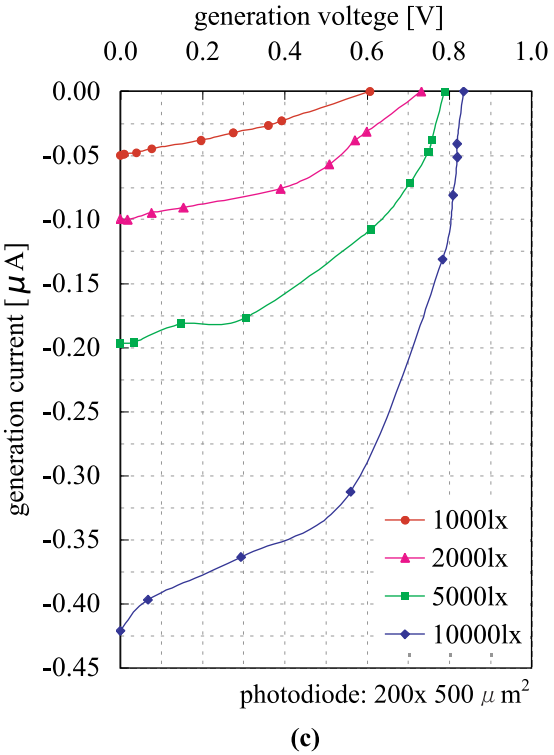


(a)



(b)

DOI: 10.1587/elex.3.287
Received May 16, 2006
Accepted June 05, 2006
Published July 10, 2006



(c)

Fig. 3. Evaluation results: (a) drive performance for full adder (b) drive performance for 7-bit counter (c) I-V characteristic of proposed solar battery

4 Conclusion

An on-chip solar battery structure to drive a conventional CMOS circuit was proposed. By the series connection of two types of photodiode that can be formed during the source drain process in conventional CMOS technology, the solar battery can be generated a high voltage of 0.6–0.83 V. From the evaluation results of the test chip, the conversion efficiency was 2.6%. In the case the 2000lx illumination, the required area of the solar battery for power consumption was 6.1 $mm^2/\mu W$. These experiment results indicate the potential of the proposed on-chip solar battery.

Acknowledgments

This work was supported by Grant-in-Aid for Scientific Research No.17560311 from Japan Society for the Promotion of Science.

DOI: 10.1587/elex.3.287
Received May 16, 2006
Accepted June 05, 2006
Published July 10, 2006